

# LCFC Confidential


## BY511/BY710 M/B Schematics Document

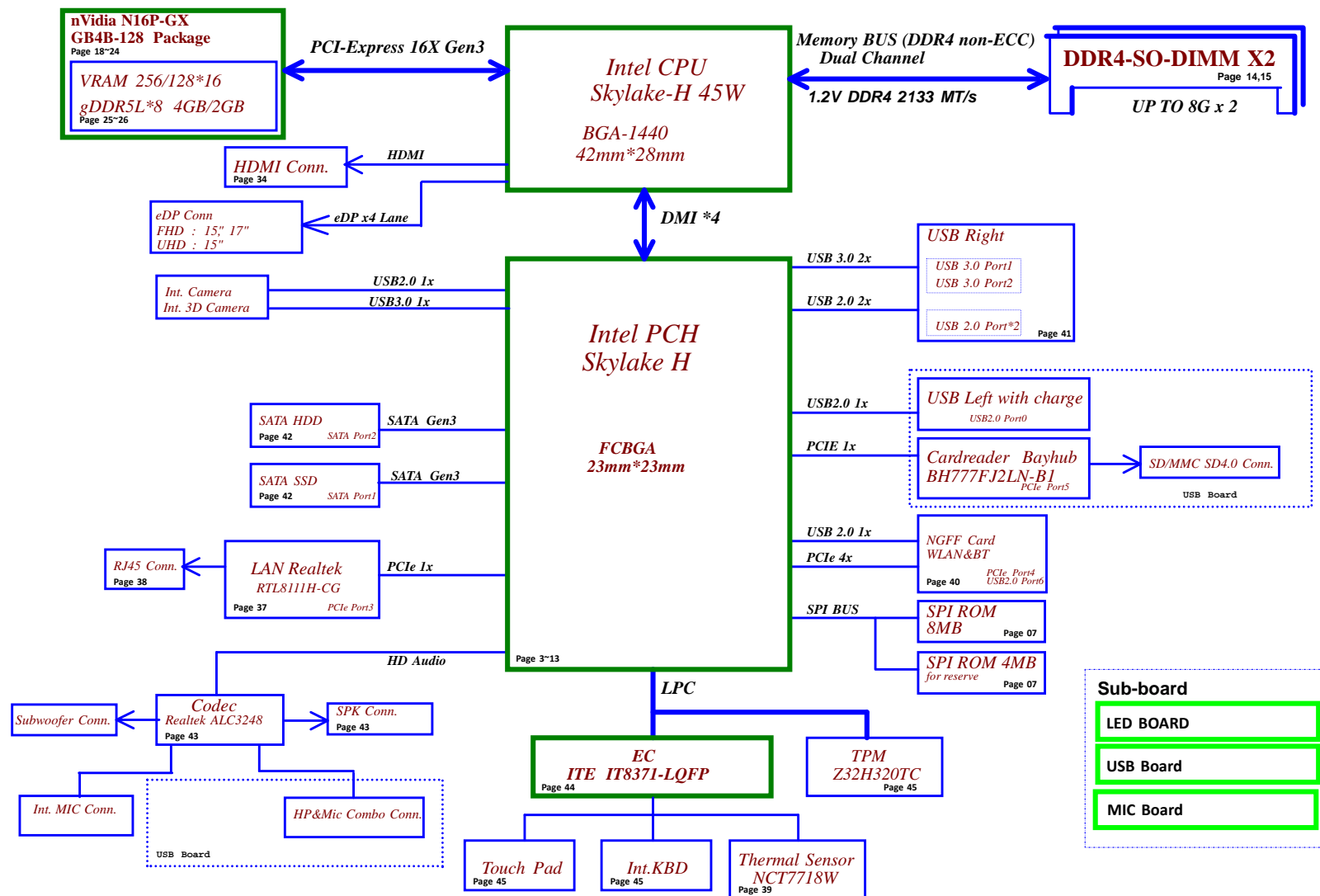
Intel Skylake H-Processor with DDR4 + NV N16P-GX GPU

MB NMA541

2015-07-31

REV:1.0

Security Classification		LC Future Center Secret Data		Title			
Issued Date	2015/02/26	Deciphered Date	2016/02/26	Cover Page			
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Voltage Rails ( 0 --> Means ON , X --> Means OFF )

Power Plane / State					
	B+	+3VALW +5VALW	+3VALW_PCH	+1.2V	+5VS +3VS +1.5VS +1.2VS +1.05VS +0.6VS CPU_CORE  +VGA_CORE +3VGS +1.8VGS +1.35VGS +0.95VGS
S0	0	0	0	0	0
S3	0	0	0	0	X
S3 Battery only	0	0	0	0	X
S5 S4/AC Only	0	0	0	X	X
S5 S4 Battery only	0	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB 2.0 Port table

Port	Function
1	RIGHT USB 2.0 (AOU)
2	LEFT USB 3.0 w/ 2.0
3	LEFT USB 3.0 w/ 2.0
4	
5	Touch Screen
6	Camera
7	
8	
9	
10	
11	Buleetooth
12	
13	
14	

PCIE 3.0 Port table

Port	Function
1	
2	SD 4.0 Card Reader
3	WLAN
4	LAN
5	
6	
7	
8	
9	M.2 SSD 4Lanes PCIe
10	M.2 SSD 4Lanes PCIe
11	M.2 SSD 4Lanes PCIe
12	M.2 SSD 4Lanes PCIe
13	
14	
15	
16	

SATA 3.0 Port table

Port	Function
1	M.2 SSD SATA Gen3
2	HDD SATA Gen3
3	
4	

USB 3.0 Port table

Port	Function
1	LEFT USB 3.0 w/ 2.0
2	LEFT USB 3.0 w/ 2.0
3	
4	
5	
6	3D Camera
7	
8	

BOM Structure Table

BOM Structure	BTO Item
@	Not stuff
14@	For 14" part
15@	For 15" part
AOAC@	AOAC support part
GIGA@	GIGA LAN Part
ME@	ME part(connector, hole)
RANKA@	For VRAM RankA part
RANKB@	For VRAM RankB part
OPT@	For GPU part
TS@	For support touch panel sku part
TPM@	For support TPM sku part
U31@	For support USB re-driver part
3D@	For support 3D camera sku part
H4@	Hynix 256Mx16 VRAM part
M4@	Micron 256Mx16 VRAM part
S4@	Samsung 256Mx16 VRAM part
S4GX4@	Samsung 256Mx16 VRAM x4pcs sku
H4GX4@	Hynix 256Mx16 VRAM x4pcs sku
M4GX4@	Micron 256Mx16 VRAM x4pcs sku
CD@	Cost down part
H4GX8@	Hynix 256Mx16 VRAM x8pcs sku
M4GX8@	Micron 256Mx16 VRAM x8pcs sku
S4GX8@	Samsung 256Mx16 VRAM x8pcs sku

SMBUS Control Table

	SOURCE	VGA	BATT	IT8586E	SODIMM	WLAN WIMAX	Thermal Sensor	PCH	TP Module	charger
EC_SMB_CK1 EC_SMB_DA1	IT8586E +3VALW	X	V	V +3VALW	X	X	X	X	X	V
EC_SMB_CK2 EC_SMB_DA2	IT8586E +3VS	V +3VGS	X	V +3VS	X	X	V +3VS	V +3VALW_PCH	X	X
PCH_SMB_CLK PCH_SMB_DATA	PCH +3VALW_PCH	X	X	X	V +3VS	V +3VS	X	V +3VALW_PCH	X	X

EC SM Bus1 address

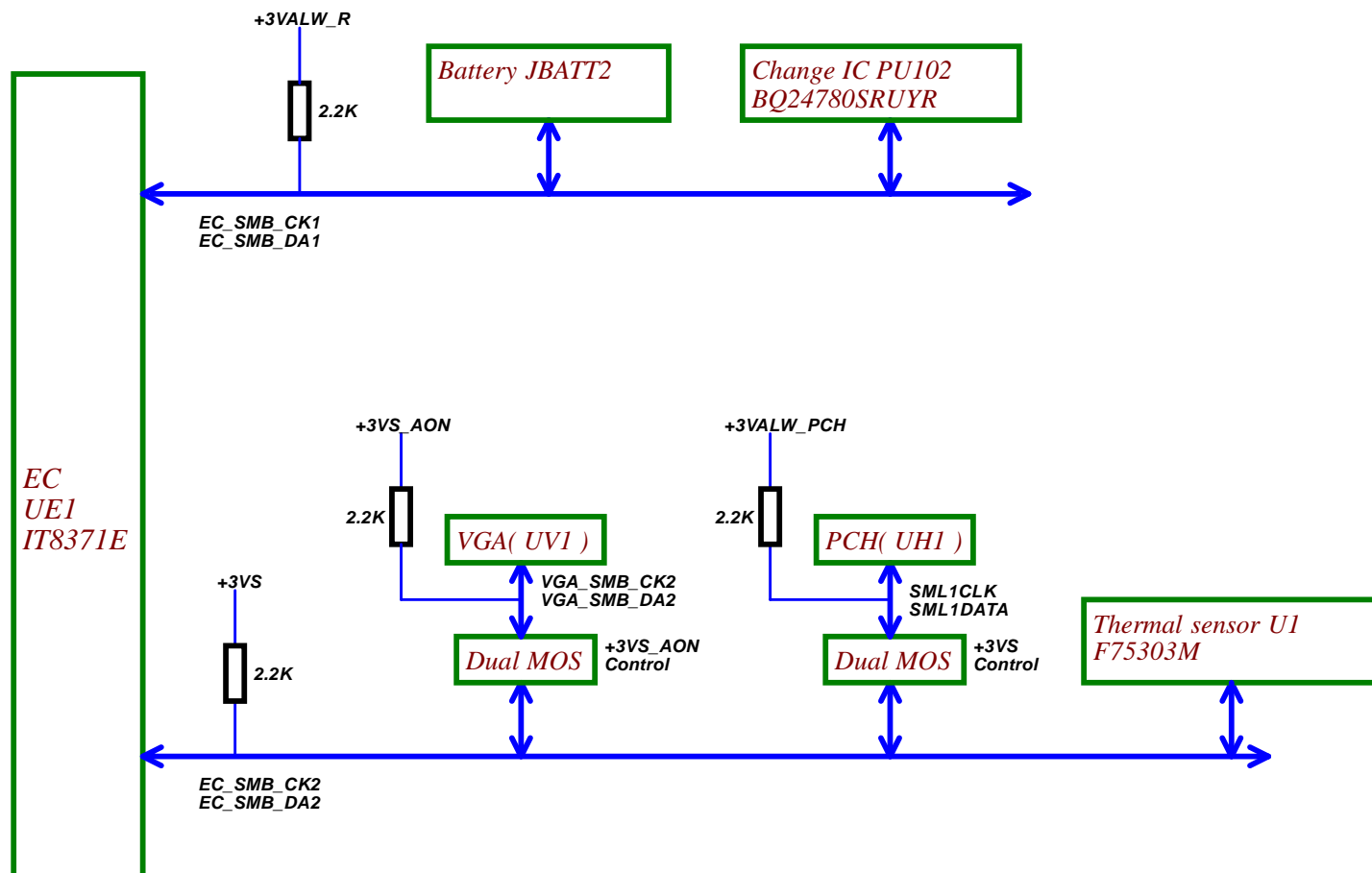
EC SM Bus2 address


PCH SM Bus address

Device	Address	Device	Address
Smart Battery	0X16	Thermal Sensor NCT7718W	1001_100xb
Charger	0001 0010 b	VGA	0x41(default)
		PCH	need to update

Device	Address
DDR DIMMA	1010 000Xb
DDR DIMMB	1010 010Xb
Wlan	Rsvd

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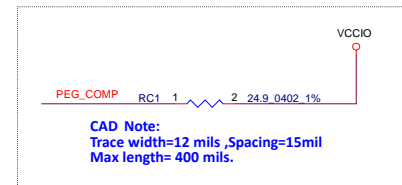
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[24] PCIE\_CRX\_GTX\_N[0..15]

[24] PCIE\_CRX\_GTX\_P[0..15]

PCIE\_CTX\_C\_GRX\_N[0..15] [24]

PCIE\_CTX\_C\_GRX\_P[0..15] [24]







HDMI D2  
HDMI D1  
HDMI D0  
HDMI CLK

[35] HDMI\_TX2+  
[35] HDMI\_TX2-  
[35] HDMI\_TX1+  
[35] HDMI\_TX1-  
[35] HDMI\_TX0+  
[35] HDMI\_TX0-  
[35] HDMI\_TXC+  
[35] HDMI\_TXC-

HDMI\_TX2+  
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HDMI\_TXC+  
HDMI\_TXC-

K36  
K37  
J35  
J34  
H37  
H36  
J37  
J38  
DDI1\_TXP[0]  
DDI1\_TXN[0]  
DDI1\_TXP[1]  
DDI1\_TXN[1]  
DDI1\_TXP[2]  
DDI1\_TXN[2]  
DDI1\_TXP[3]  
DDI1\_TXN[3]

D27  
E27  
H34  
H33  
F37  
G38  
F34  
F35  
E37  
E36  
DDI1\_AUXP  
DDI1\_AUXN  
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DDI2\_TXN[3]

F26  
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C34  
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B36  
B34  
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A27  
B27  
DDI3\_AUXP  
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SKYLAKE-H-CPU\_BGA1440

UC1D SKYLAKE\_HALO

BGA1440

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EDP\_AUXP  
EDP\_AUXN

EDP\_DISP\_UTIL

EDP\_RCOMP

PROC\_AUDIO\_CLK  
PROC\_AUDIO\_SDI  
PROC\_AUDIO\_SDO

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### COMPENSATION PU FOR eDP

CAD Note:Trace width=20 mils ,Spacing=25mil,  
Max length=100 mils.

20\_0402\_1% 1 2 RC180

Place near CPU.

Need create 5% P/N

RH762 33\_0402\_5%

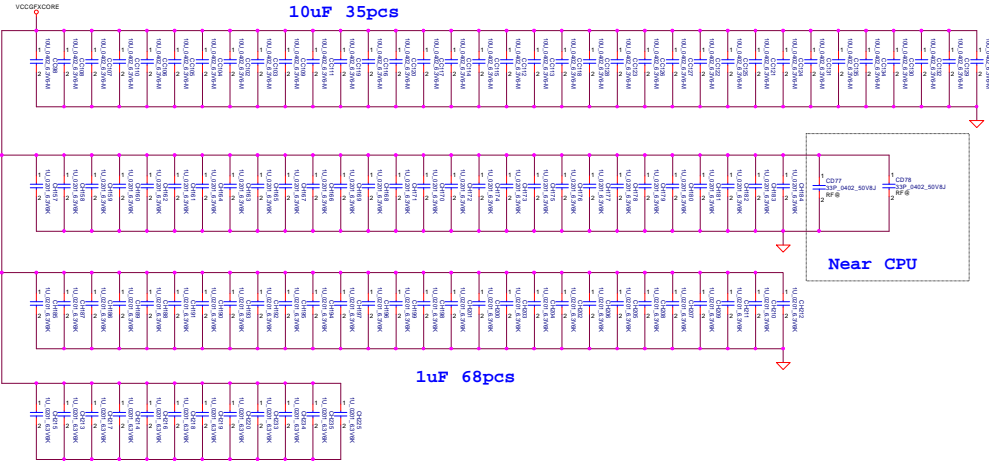
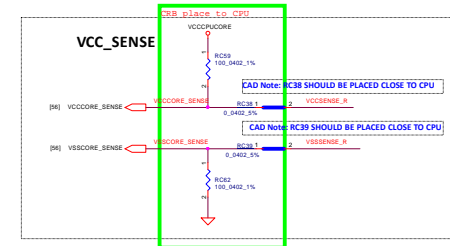
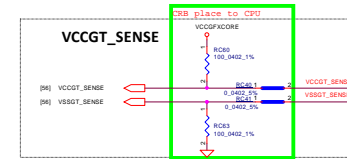
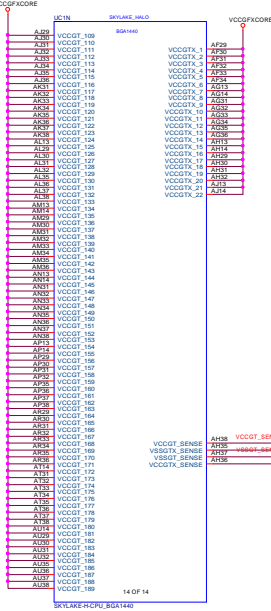
CH264 10P\_0402\_50V8J


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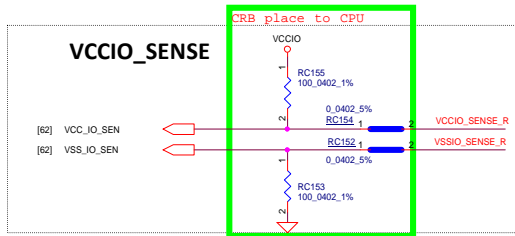
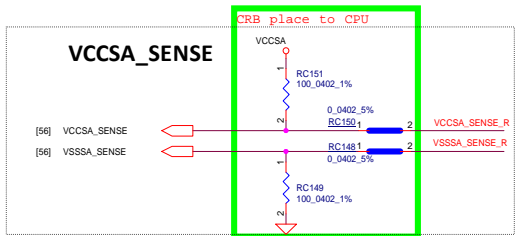
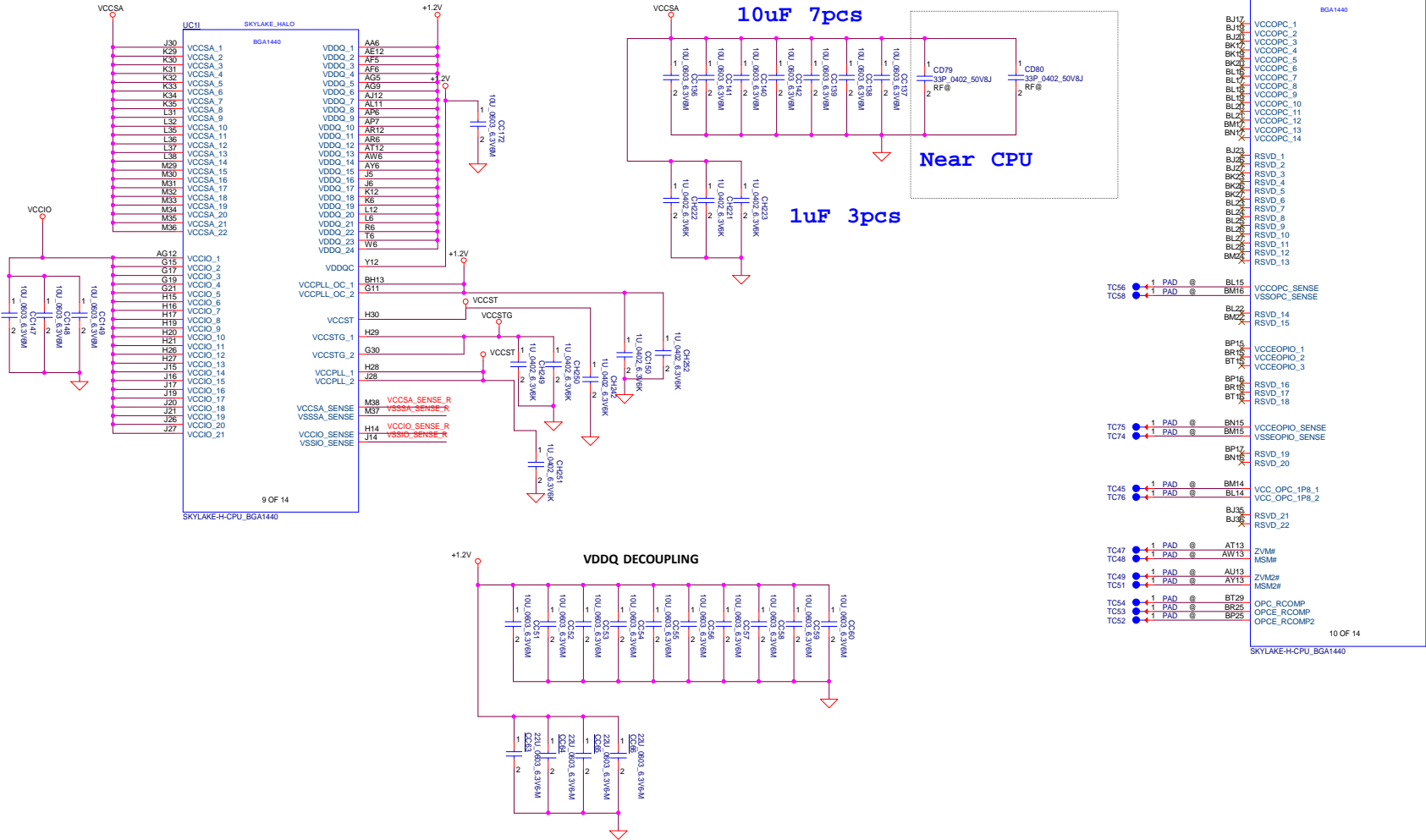
Title		CPU (4/7) eDP, DDI	
Size	Document Number	Rev	0.3
Custom	BY511/BY710		
Date:	Friday, July 31, 2015	Sheet	8 of 66

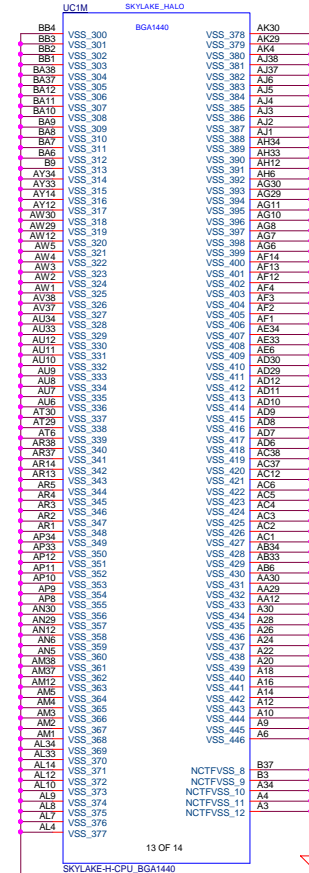


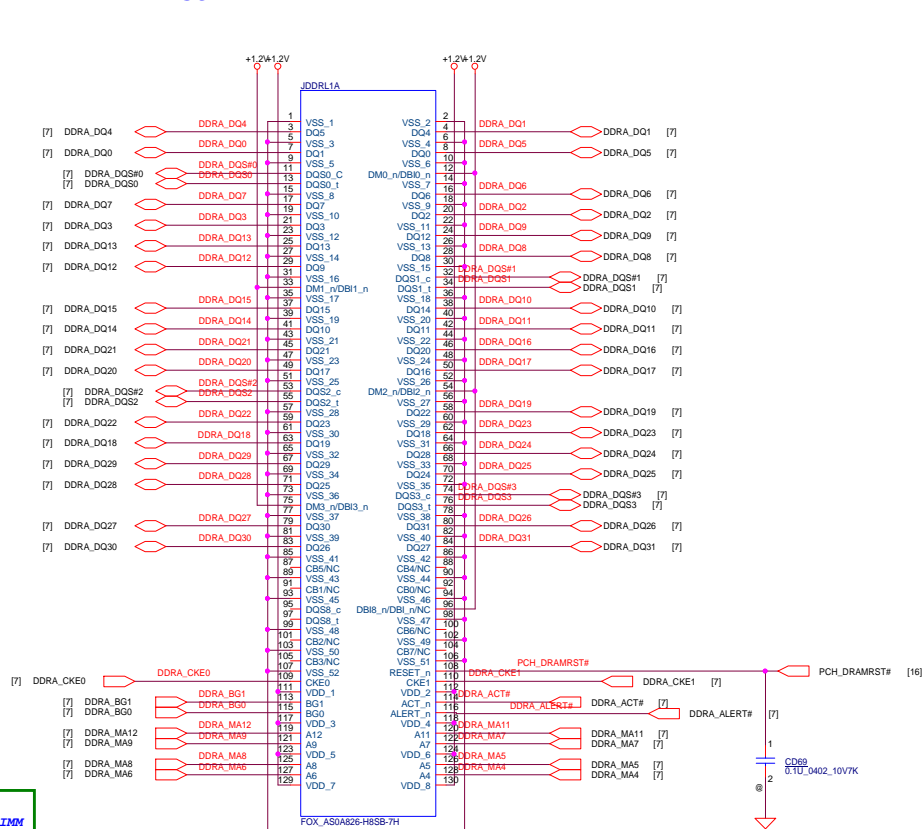




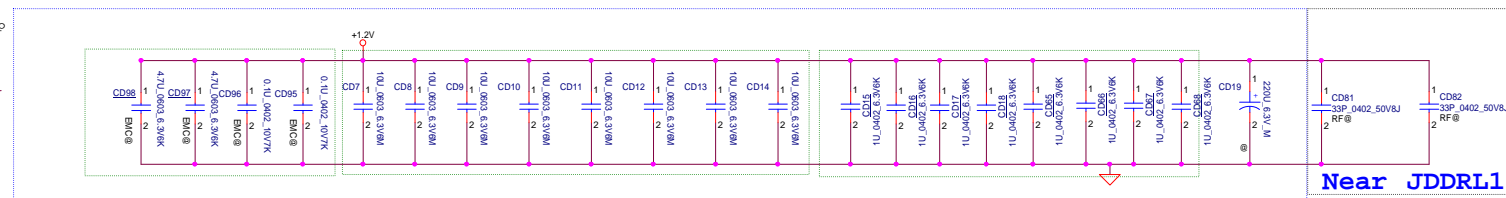
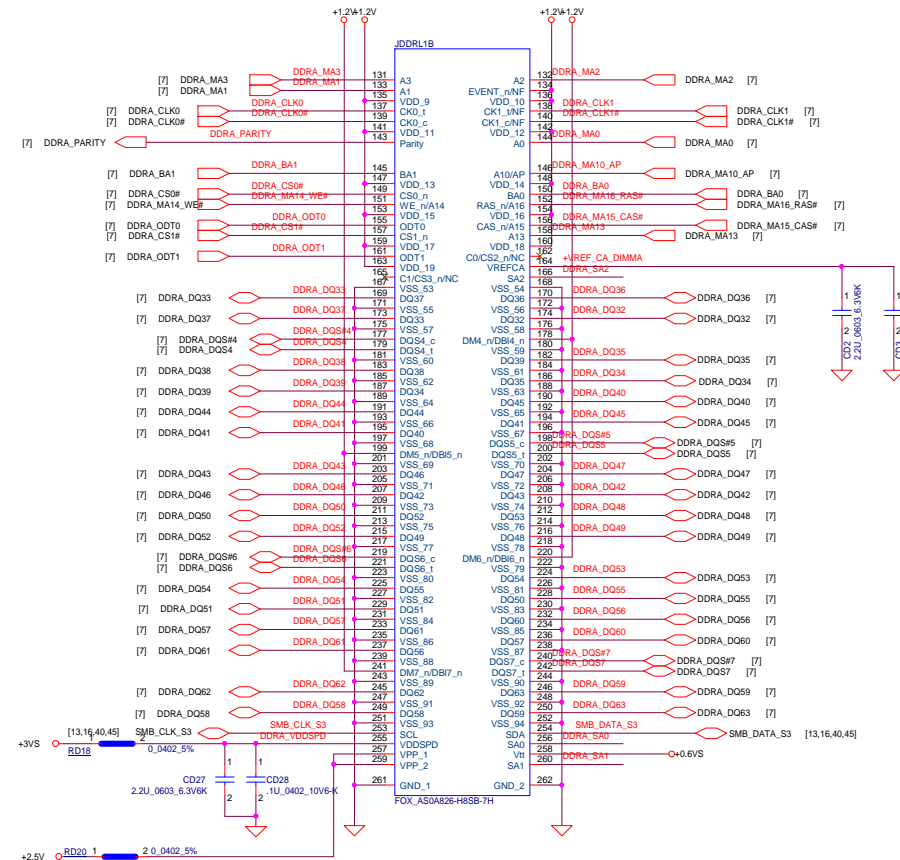
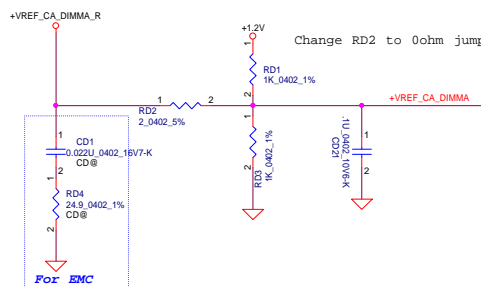
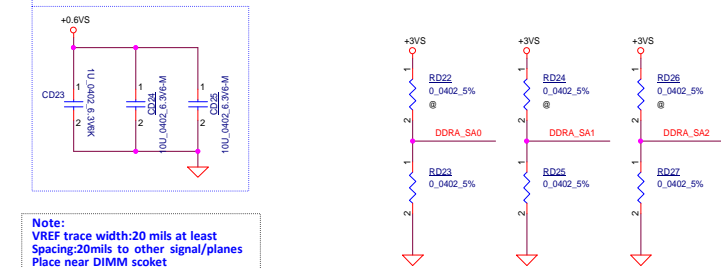
Security Classification	LC Future Center Secret Data		Title
Issued Date	2015/02/26	Deciphered Date	2016/02/26
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Size D	Document Number	BY511/BY710	






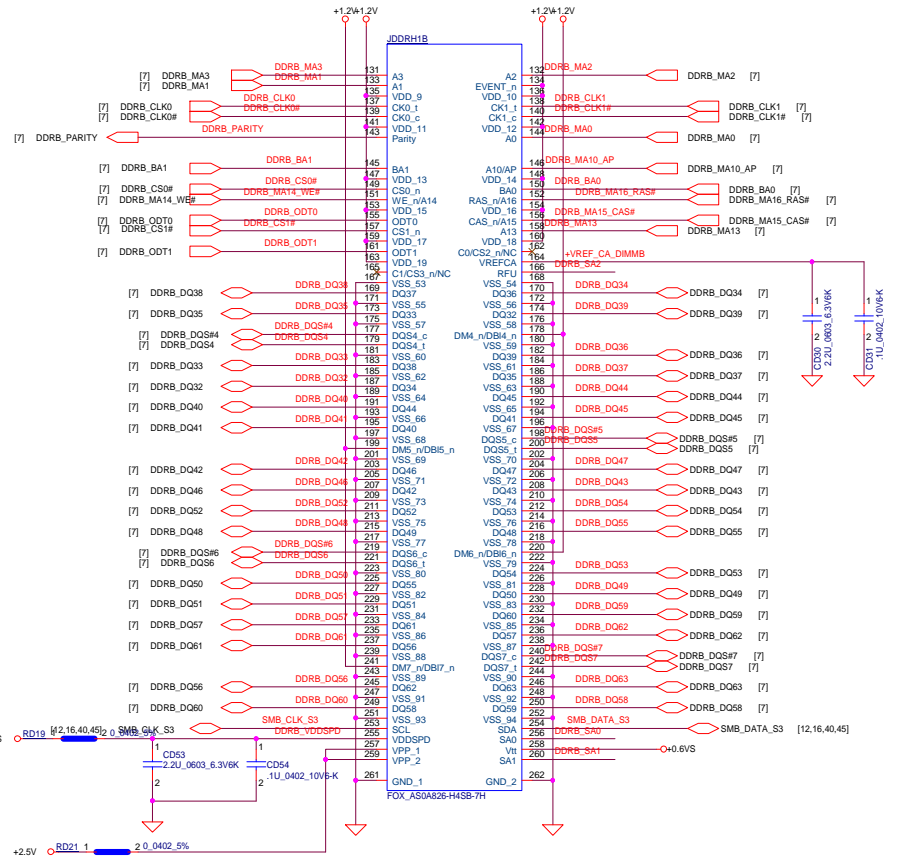
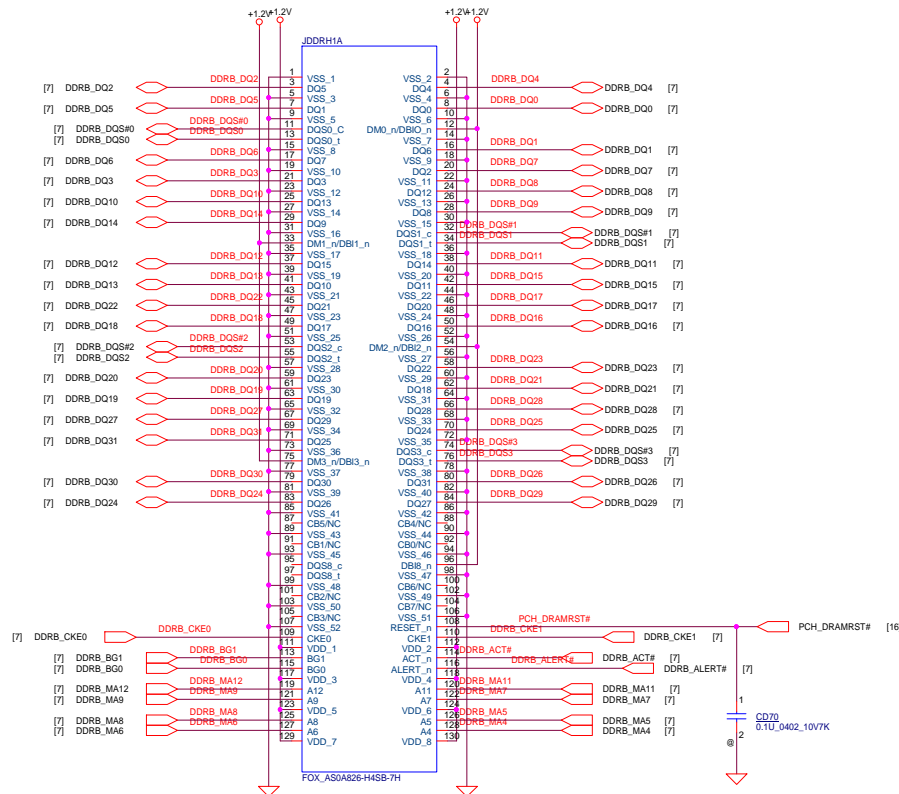
**DDR4 SO-DIMM A**

SPD Address = 0H



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				Date: Friday, July 31, 2015	Sheet 12 of 66

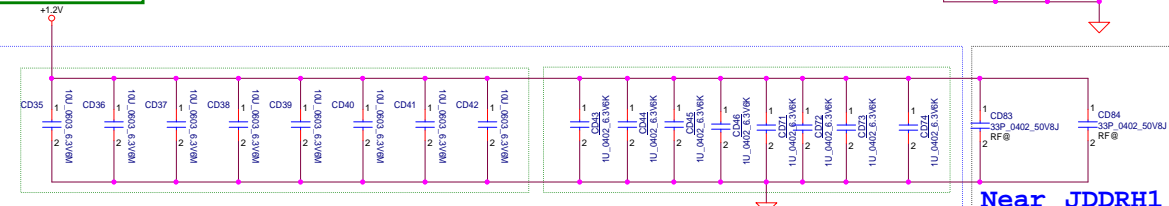
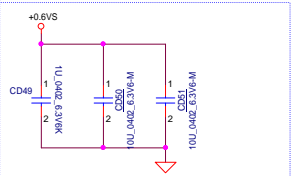
# DDR4 SO-DIMM B



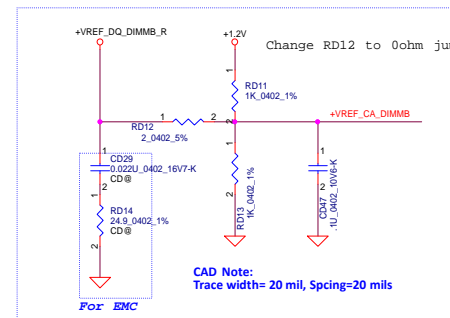
SPD Address = 2H

Layout Note:  
Place near DIMM

Layout Note:  
Place near DIMM



Near JDDRH1

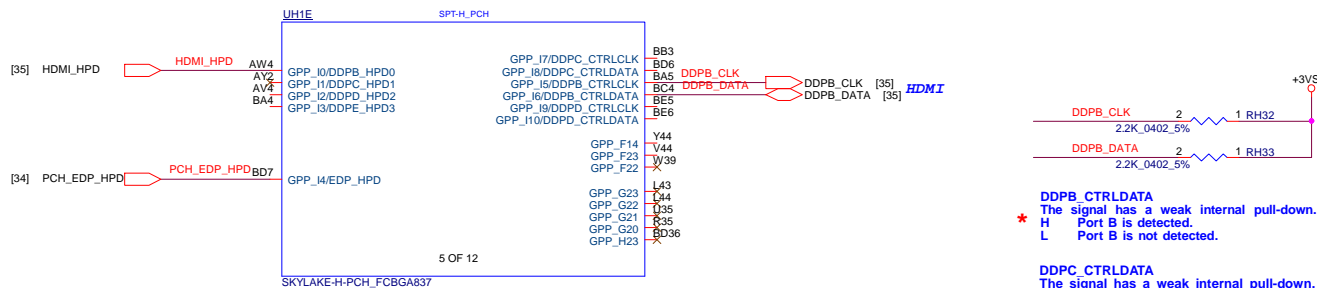



CAD Note:  
Trace width = 20 mil, Spacing=20 mils

For EMC





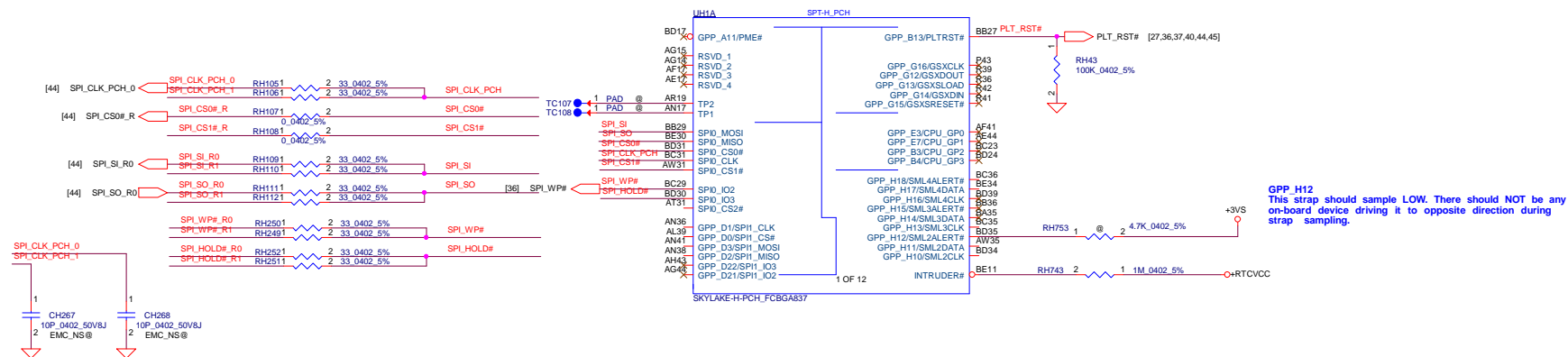


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Issued Date	2015/02/26	Deciphered Date	2016/02/26	PCH (2/9) USB3/GPPAEFGHI		
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				Date: Friday, July 31, 2015	Sheet 15 of 66	Rev 0.3

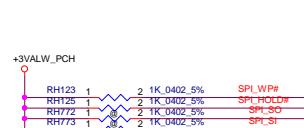




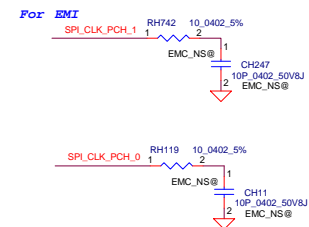
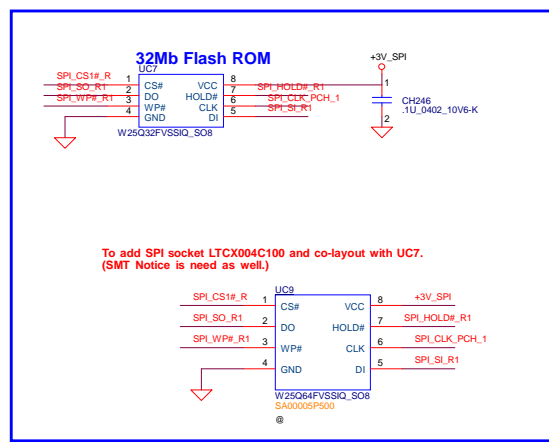
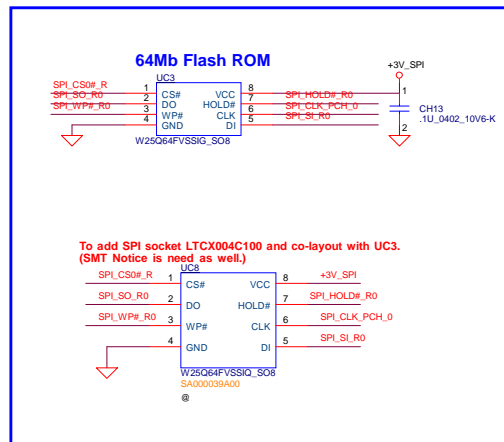


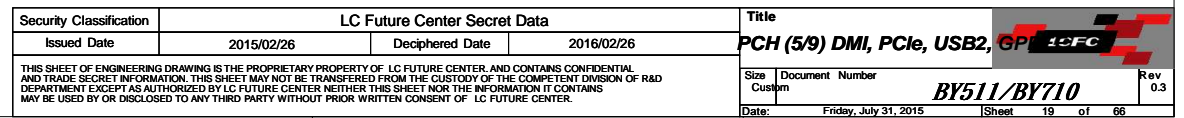


SPI0\_MOSI  
SPI0\_MISO  
This signal has an internal pull-up.  
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

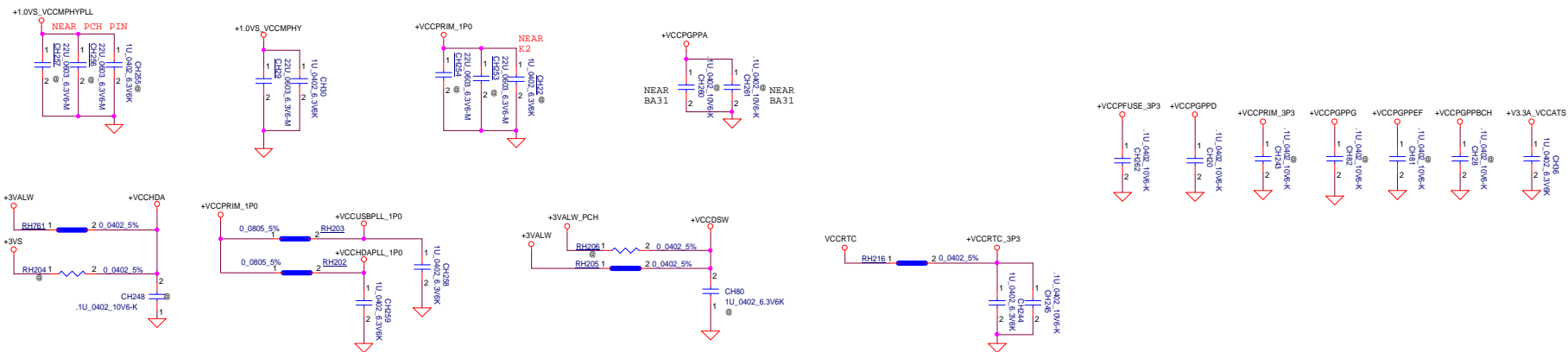


- 1. If support DS3, connect to +3VS and don't support EC mirror code;
- \* 2. If don't support DS3, connect to +3VALW\_PCH and support EC mirror code









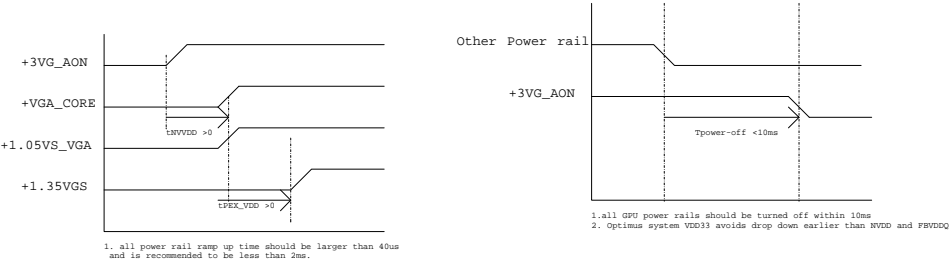
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N16P-GX GPIO

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	FB Enable for GC6 2.0
GPIO1	OUT	N/A	
GPIO2	OUT	N/A	
GPIO3	OUT	N/A	
GPIO4	OUT	N/A	
GPIO5	OUT	N/A	GPU power sequencing---3V3_MAIN_EN
GPIO6	IN	-	GPU wake signal for GC6 2.0
GPIO7	OUT	N/A	
GPIO8	IN	-	System side PCIe reset Monitor
GPIO9	I/O	-	VGA_ALERT#
GPIO10	OUT	-	Memory VREF Control (100K pull Down)
GPIO11	OUT	-	GPU Core VDD PWM control signal
GPIO12	IN	-	AC Power Detect Input (10K pull High)
GPIO13	OUT	-	Phase Shedding
GPIO14	IN	N/A	
GPIO15	IN	N/A	
GPIO16	IN	N/A	
GPIO17	IN	N/A	
GPIO18	IN	N/A	
GPIO19	IN	N/A	
GPIO20		N/A	
GPIO21	OUT	-	GPU PCIe self-reset control
OVERT	I/O	-	Active Low Thermal Catastrophic Over Temperature

N16P-GX Power Sequence



Performance Mode P0 TDP at Tj = 102 C\* (DDR5)

Products	GPU (4) (W)	Mem (1.5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)			FBVDD (1.35V) (A)		FBVDDQ (GPU+Mem) (1.35V) (A)		PCI Express (1.05V) (6) (A)		I/O and PLLVDD (1.05V) (A)		Other (3.3V) (A)	
N16P-GX 128bit 2GB DDR5	50	3.27	2505	TBD	51.1	TBD	3.46	4.67	8.75	11.81	TBD	TBD	2.57	2.7	0.34	TBD

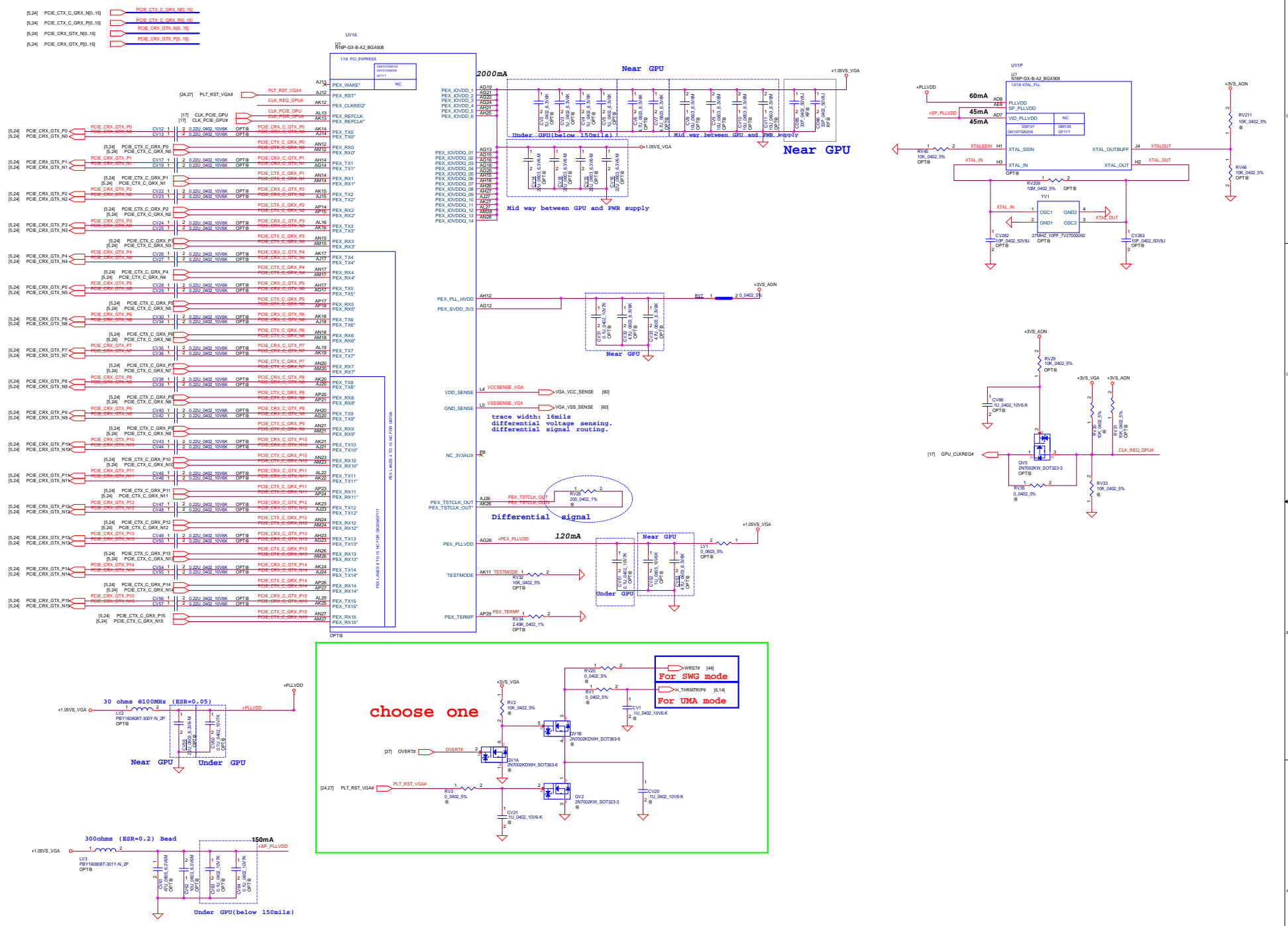
N16P-GX Multi-level Straps

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

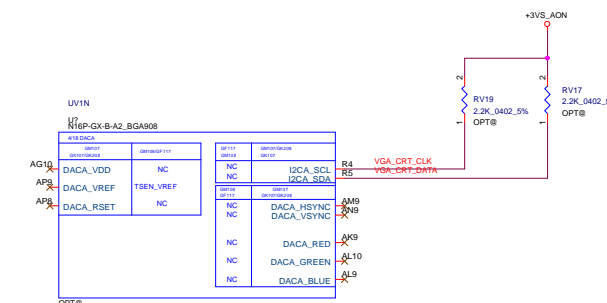
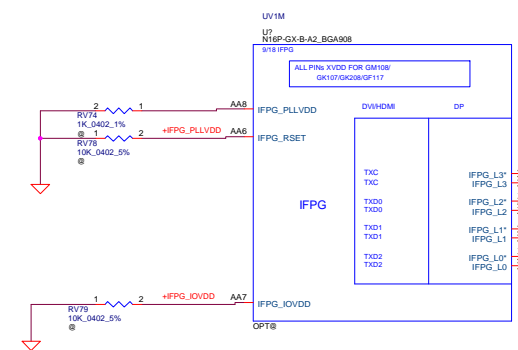
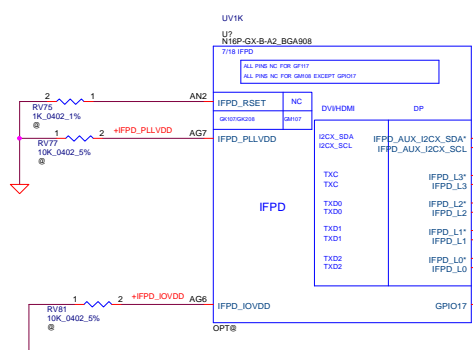
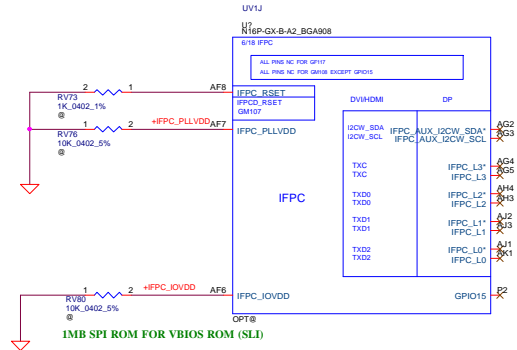
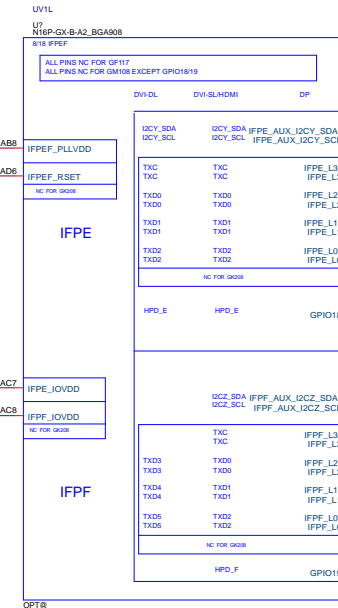
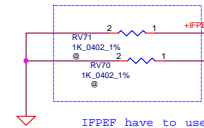
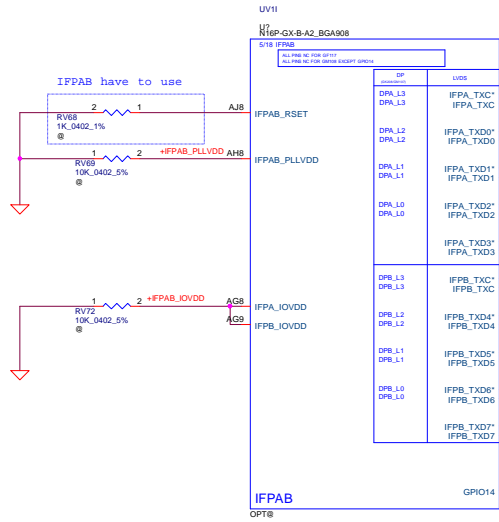
SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

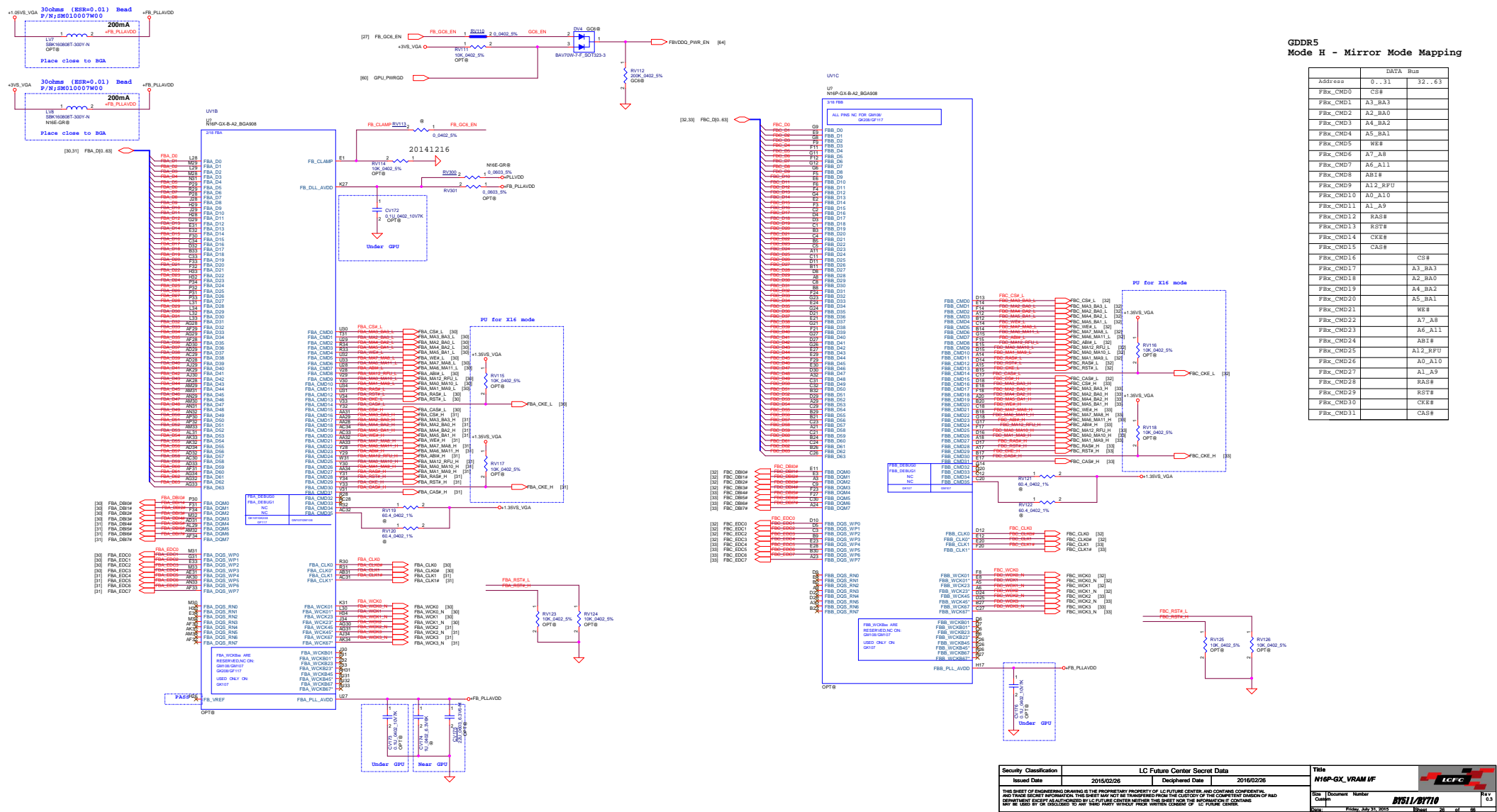
N16P-GX Binary Straps

Physical Strapping pin	Power Rail	Strap Mapping
ROM_SCLK	+3VGS	SMB_ALT_ADDR
ROM_SI	+3VGS	SUB_VENDOR
ROM_SO	+3VGS	VGA_DEVICE
STRAP0	+3VGS	RAM_CFG[0]
STRAP1	+3VGS	RAM_CFG[1]
STRAP2	+3VGS	RAM_CFG[2]
STRAP3	+3VGS	RAM_CFG[3]
STRAP4	+3VGS	PCIE_MAX_SPEED






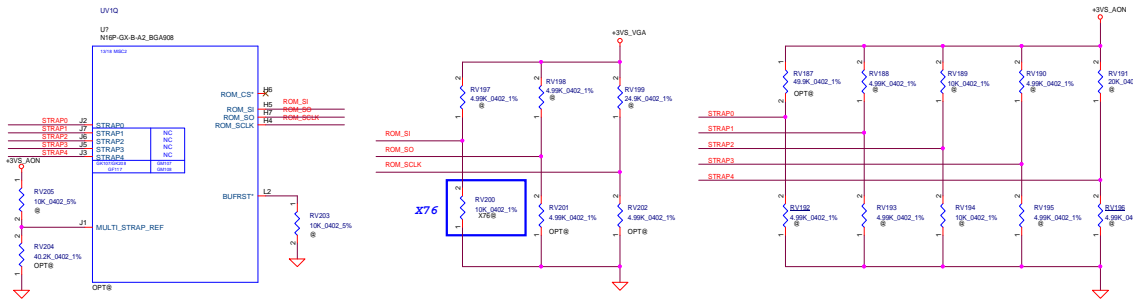




GDDR5  
Mode H - Mirror Mode Mapping

Address	DATA	Bus
Fbx_CMD0	CS#	32..63
Fbx_CMD1	A3_BA3	
Fbx_CMD2	A2_BA0	
Fbx_CMD3	A4_BA2	
Fbx_CMD4	A5_BA1	
Fbx_CMD5	WE#	
Fbx_CMD6	A7_A8	
Fbx_CMD7	A6_A11	
Fbx_CMD8	AB1#	
Fbx_CMD9	A12_RFU	
Fbx_CMD10	A0_A10	
Fbx_CMD11	A1_A9	
Fbx_CMD12	RAS#	
Fbx_CMD13	RST#	
Fbx_CMD14	CKE#	
Fbx_CMD15	CAS#	
Fbx_CMD16	CS#	
Fbx_CMD17	A3_BA3	
Fbx_CMD18	A2_BA0	
Fbx_CMD19	A4_BA2	
Fbx_CMD20	A5_BA1	
Fbx_CMD21	WE#	
Fbx_CMD22	A7_A8	
Fbx_CMD23	A6_A11	
Fbx_CMD24	AB1#	
Fbx_CMD25	A12_RFU	
Fbx_CMD26	A0_A10	
Fbx_CMD27	A1_A9	
Fbx_CMD28	RAS#	
Fbx_CMD29	RST#	
Fbx_CMD30	CKE#	
Fbx_CMD31	CAS#	

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Doc No.		Doc Rev.		Doc Ver.		Doc Rev.	
Doc No.		Doc Rev.		Doc Ver.		Doc Rev.	



GPU	FB Memory (GDDR5)	ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N16P-GX	Samsung	K4G020325PD-FC03 128X16	PD 5K						
		K4G041325PC-RC03 256X16	PD 20K						
	Hynix	H5GC2H24BFR-T2C 128X16	PD 10K						
		H5GC4H24AJR-T2C 256X16	PD 34.8K						
	Micron	EDW2032BBBQ-6A-F 128X16	PD 30.1K						
		EDW4032BABQ-60-F 256X16	PD 24.9K						

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VGS	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	+3VGS	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VGS	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VGS	Reserved(keep pull-up and pull-down footprint and stuff 50kOhm pull-up)			
STRAP1	+3VGS	Reserved(keep pull-up and pull-down footprint and not stuff by default)			
STRAP2	+3VGS				
STRAP3	+3VGS				
STRAP4	+3VGS				

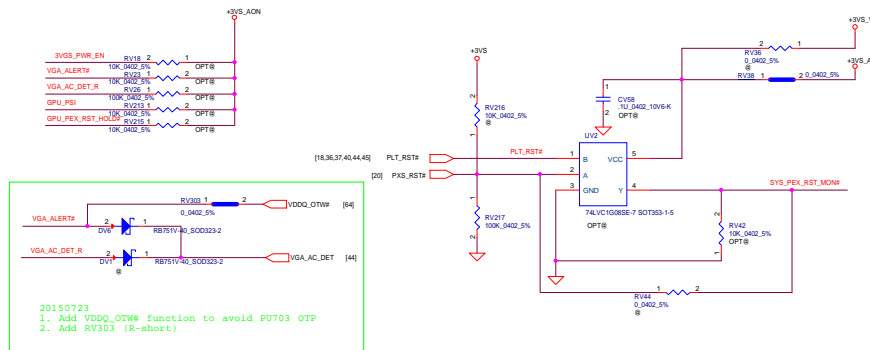
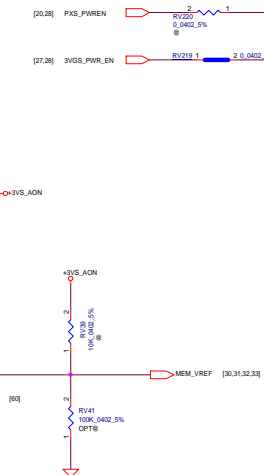
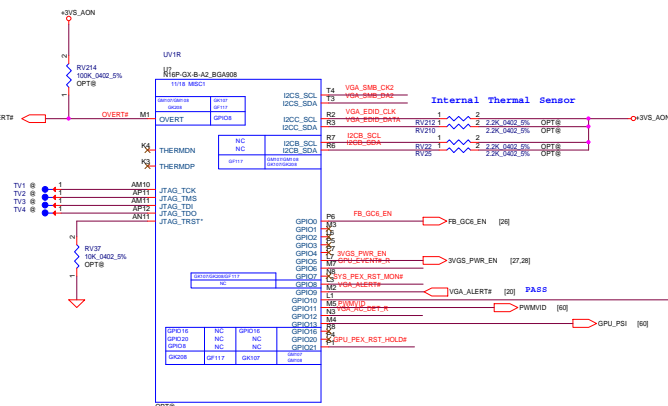
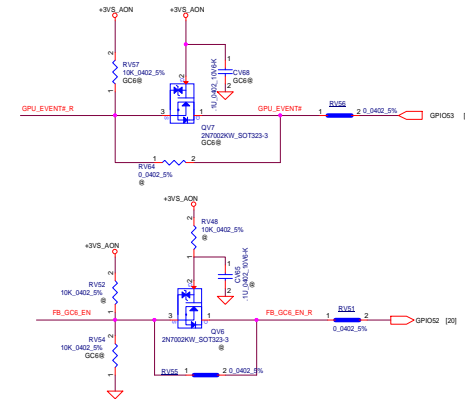
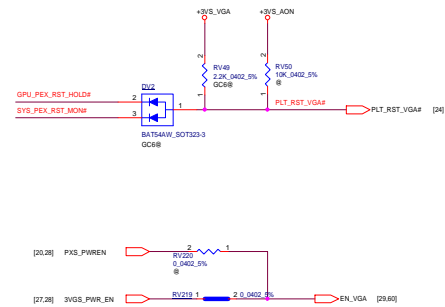
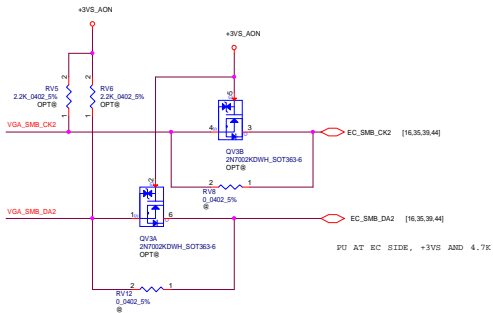
Resistor Values	Pull-up to +3VGS	Pull-down to Gnd
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

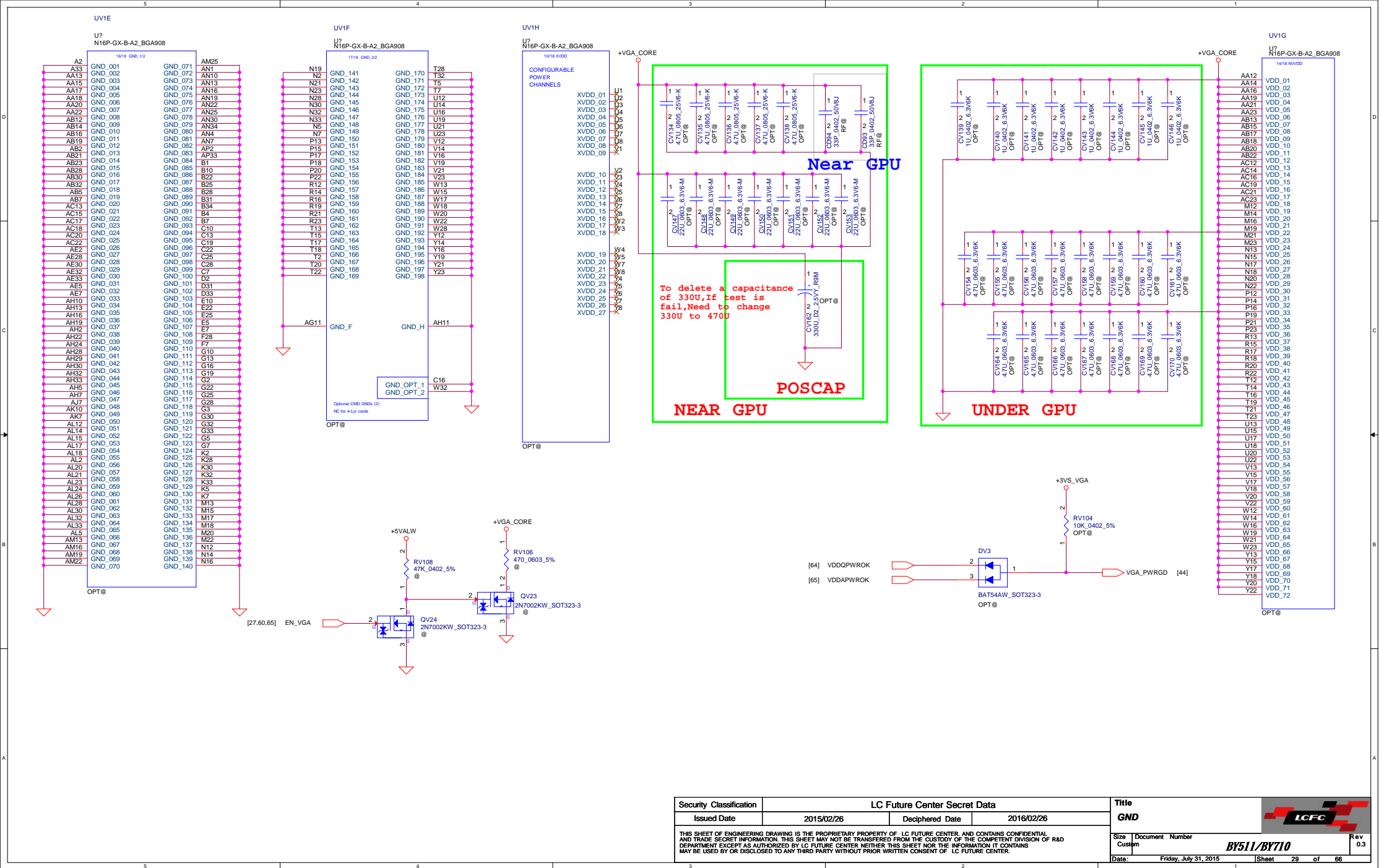
SMBUS_ALT_ADDR	
0	0x6E (Default)
1	0x6C (Multi-GPU usage)


VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)



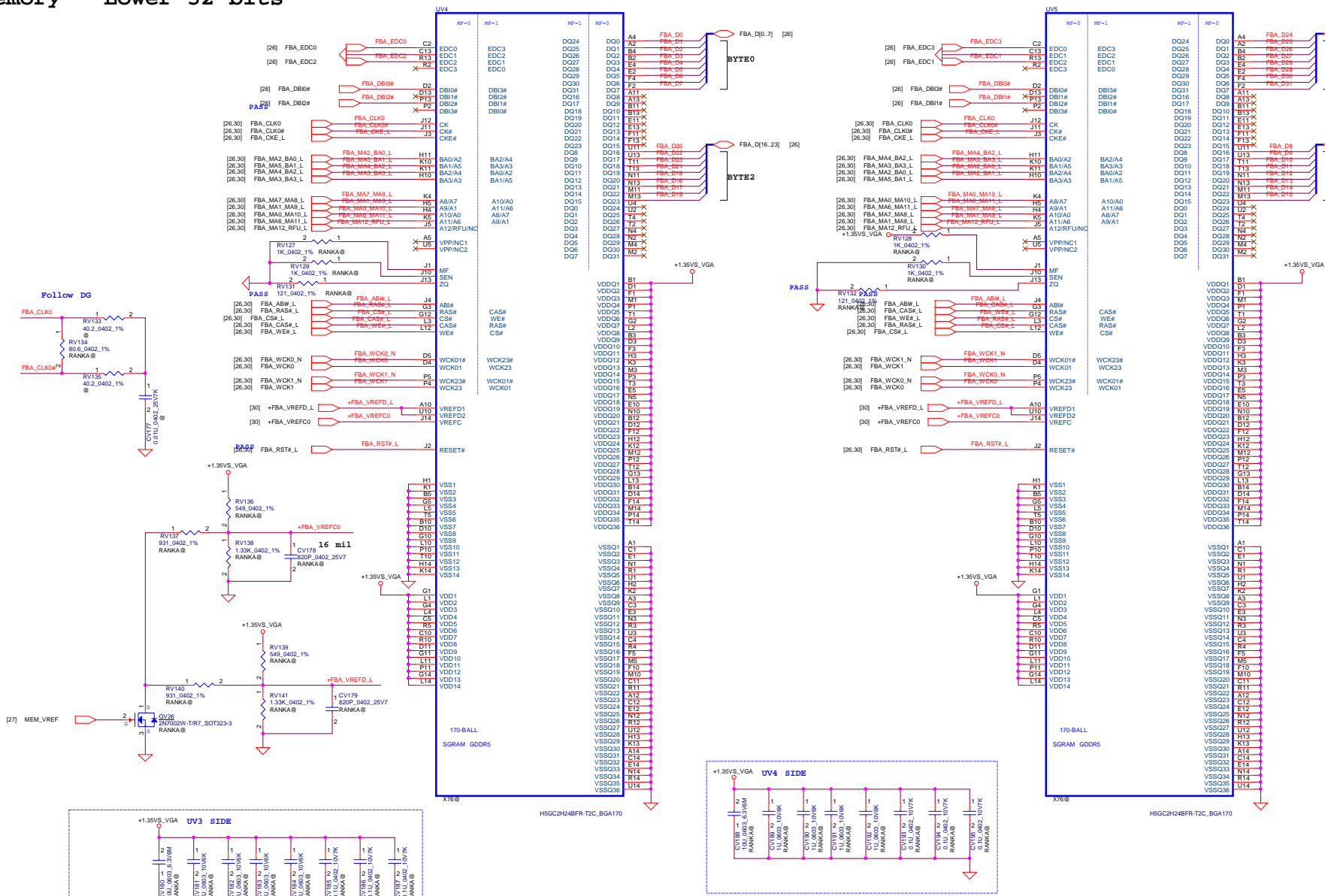
20150723  
1. Add VDDQ\_OTW# function to avoid PU703 OTP  
2. Add RV303 (R-short)





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				Date:	Friday, July 31, 2015	Sheet 29 of 66

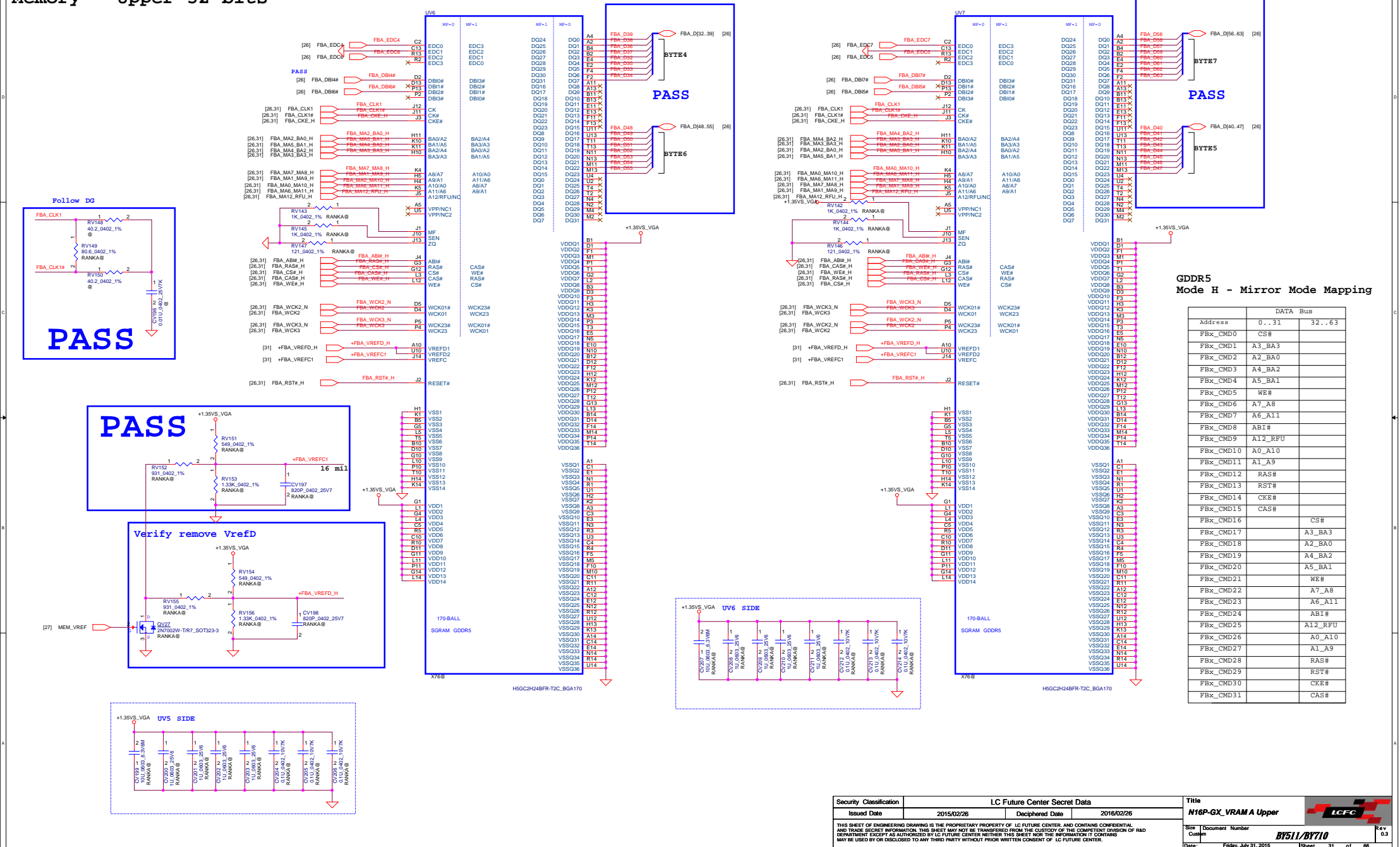
Memory - Lower 32 bits



GDDR5 Mode H - Mirror Mode Mapping

Address	DATA Bus
FbxCMD0	CS#
FbxCMD1	A3_BA3
FbxCMD2	A2_BA2
FbxCMD3	A4_BA2
FbxCMD4	A5_BA1
FbxCMD5	WE#
FbxCMD6	A7_A8
FbxCMD7	A6_A11
FbxCMD8	AB1#
FbxCMD9	A12_RFU
FbxCMD10	A0_A10
FbxCMD11	A1_A9
FbxCMD12	RAS#
FbxCMD13	RST#
FbxCMD14	CKE#
FbxCMD15	CAS#
FbxCMD16	CS#
FbxCMD17	A3_BA3
FbxCMD18	A2_BA0
FbxCMD19	A4_BA2
FbxCMD20	A5_BA1
FbxCMD21	WE#
FbxCMD22	A7_A8
FbxCMD23	A6_A11
FbxCMD24	AB1#
FbxCMD25	A12_RFU
FbxCMD26	A0_A10
FbxCMD27	A1_A9
FbxCMD28	RAS#
FbxCMD29	RST#
FbxCMD30	CKE#
FbxCMD31	CAS#

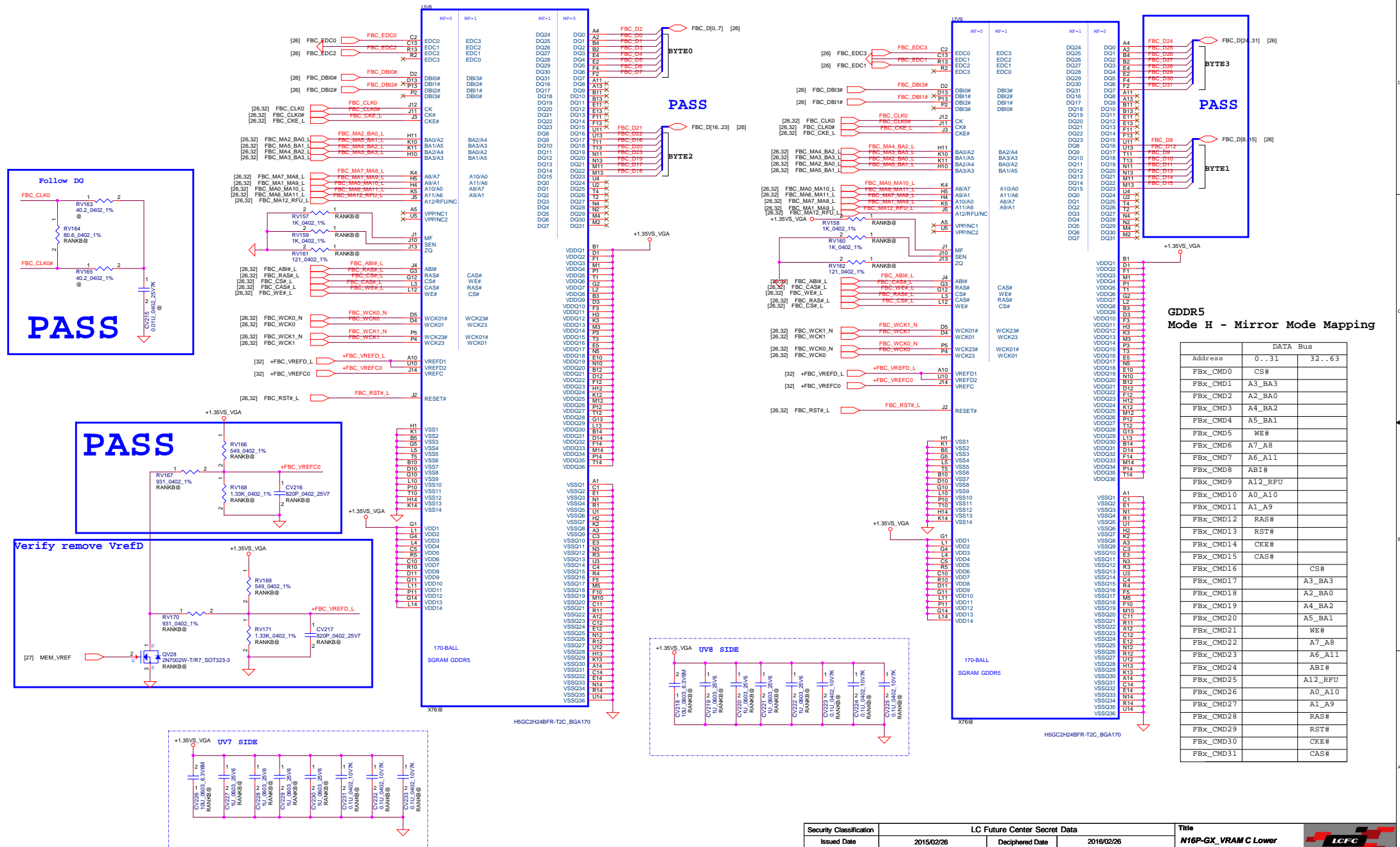
Memory - Upper 32 bits



	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	AB1#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21	WE#	
FBx_CMD22	A7_A8	
FBx_CMD23	A6_A11	
FBx_CMD24	AB1#	
FBx_CMD25	A12_RFU	
FBx_CMD26	A0_A10	
FBx_CMD27	A1_A9	
FBx_CMD28	RAS#	
FBx_CMD29	RST#	
FBx_CMD30	CKE#	
FBx_CMD31	CAS#	

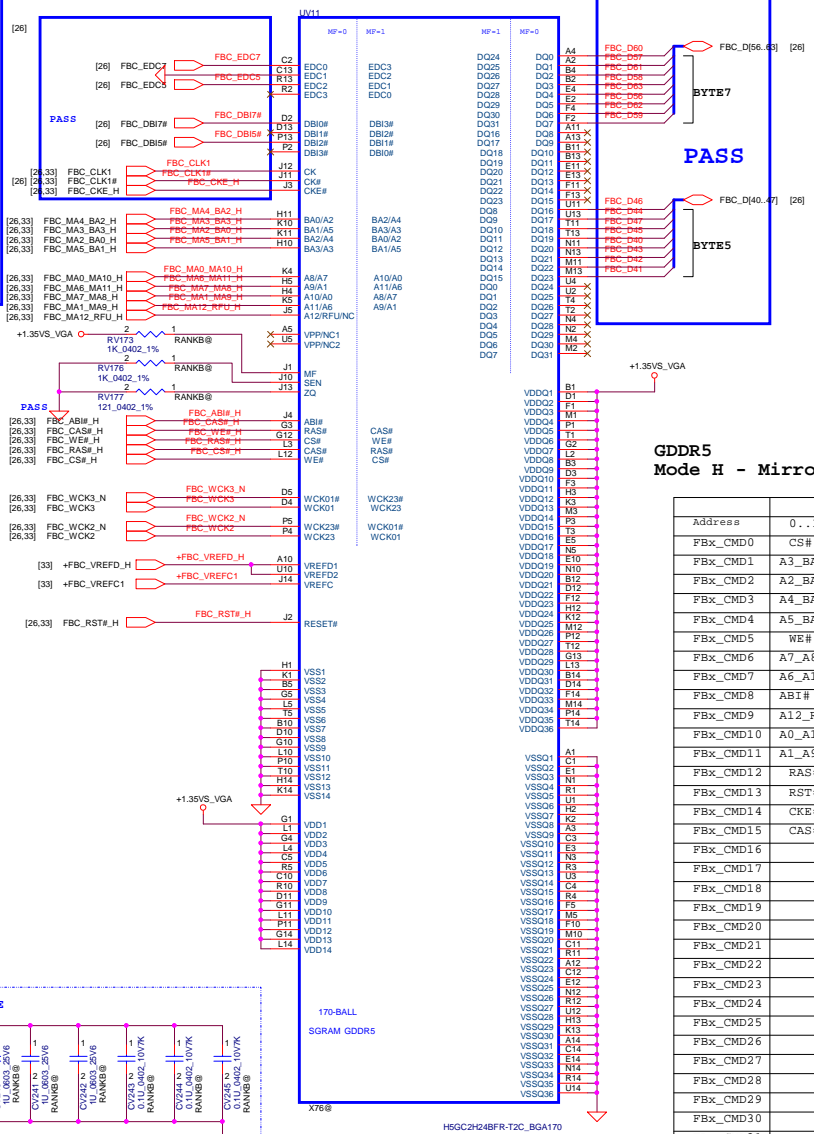
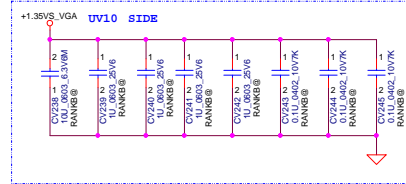
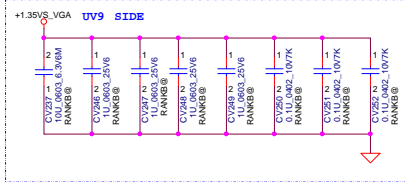
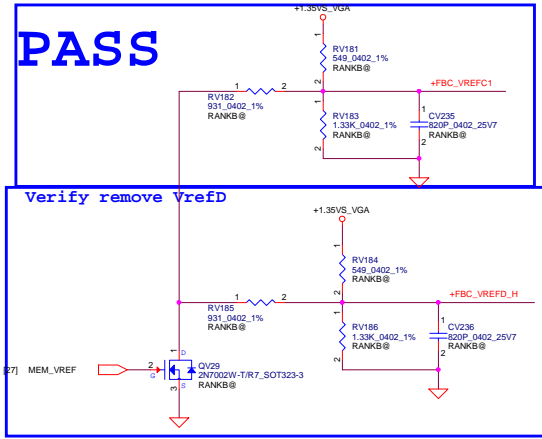
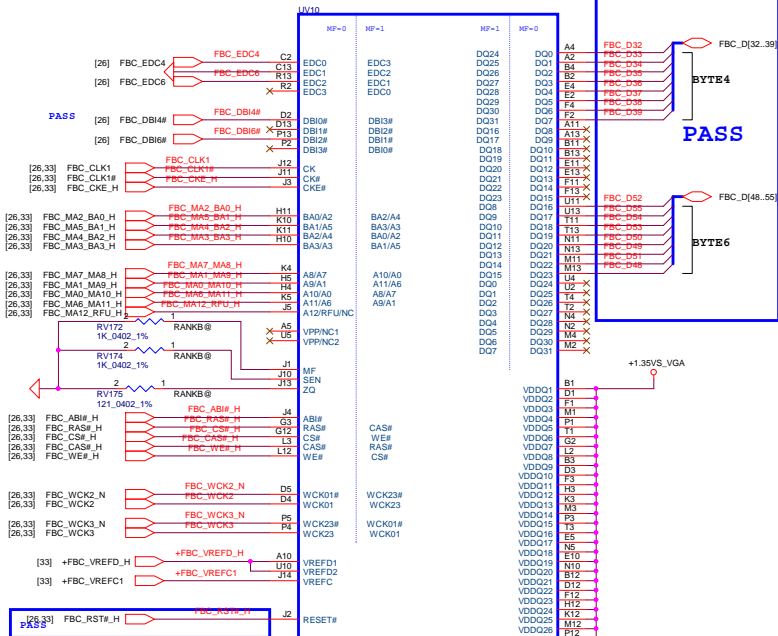
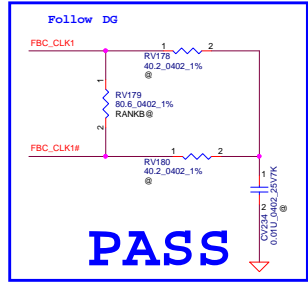


# Memory Partition C - Lower 32 bits





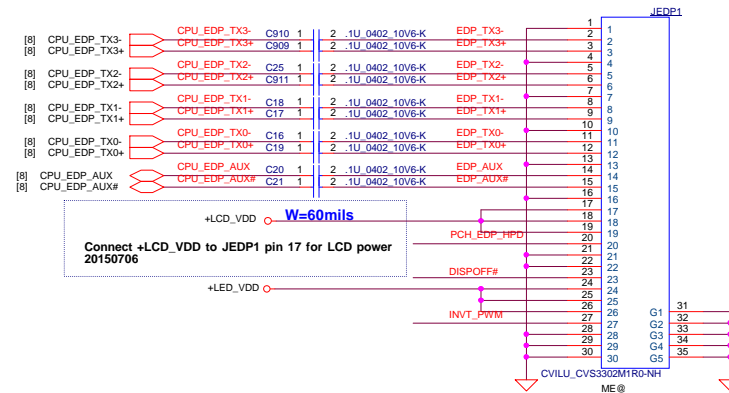
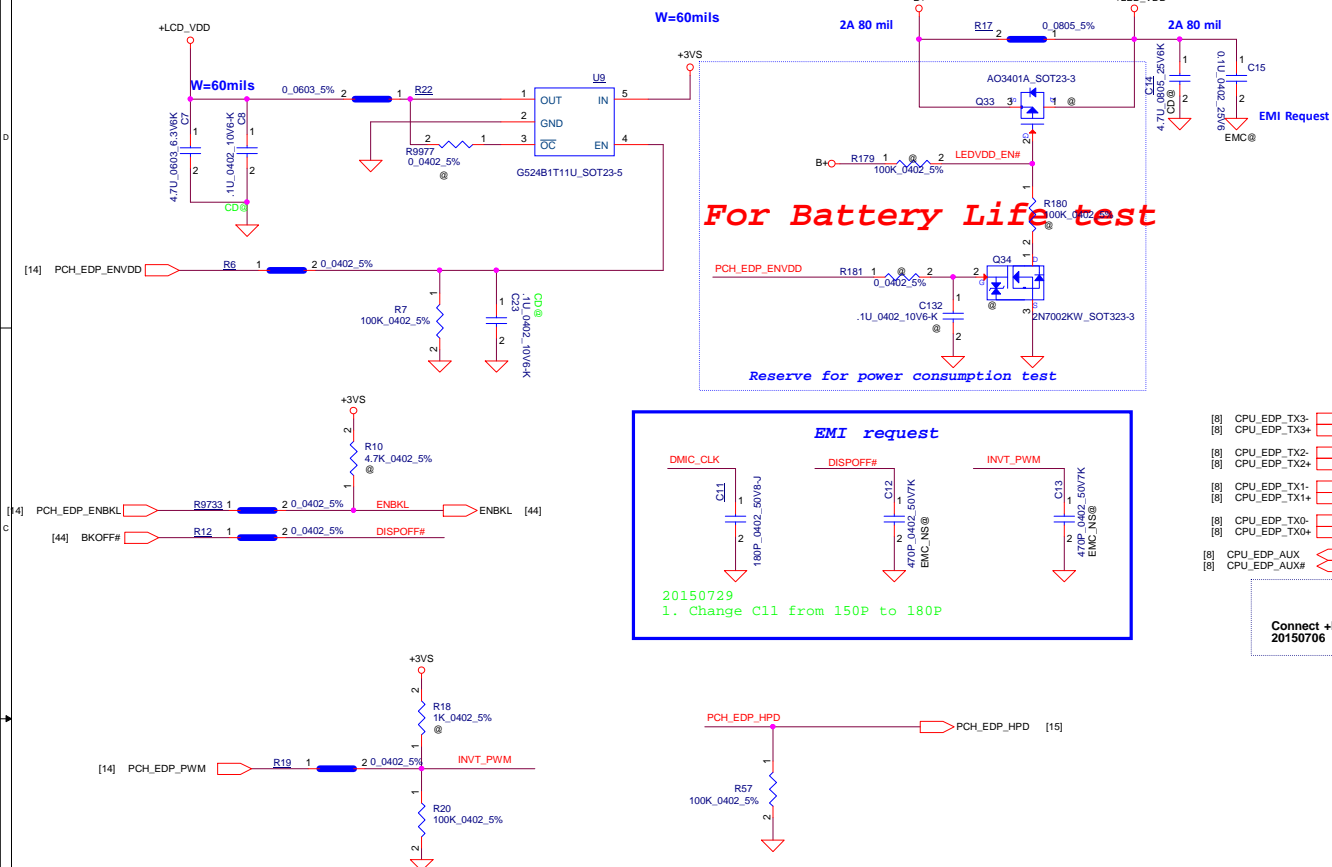
### Memory Partition C - Upper 32 bits



GDDR5  
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBX_CMD0	CS#	
FBX_CMD1	A3_BA3	
FBX_CMD2	A2_BA0	
FBX_CMD3	A4_BA2	
FBX_CMD4	A5_BA1	
FBX_CMD5	WE#	
FBX_CMD6	A7_A8	
FBX_CMD7	A6_A11	
FBX_CMD8	ABI#	
FBX_CMD9	A12_RFU	
FBX_CMD10	A0_A10	
FBX_CMD11	A1_A9	
FBX_CMD12	RAS#	
FBX_CMD13	RST#	
FBX_CMD14	CKE#	
FBX_CMD15	CAS#	
FBX_CMD16		CS#
FBX_CMD17		A3_BA3
FBX_CMD18		A2_BA0
FBX_CMD19		A4_BA2
FBX_CMD20		A5_BA1
FBX_CMD21		WE#
FBX_CMD22		A7_A8
FBX_CMD23		A6_A11
FBX_CMD24		ABI#
FBX_CMD25		A12_RFU
FBX_CMD26		A0_A10
FBX_CMD27		A1_A9
FBX_CMD28		RAS#
FBX_CMD29		RST#
FBX_CMD30		CKE#
FBX_CMD31		CAS#

# LCD POWER CIRCUIT



## CMOS Camera

20150727\_Add C10019  
by EMC suggestion  
C10019 close to JCCD

Close to JCCD Pin2


For EMI

## Touch Screen

For EMI

For EMI

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Title		
eDP/CMOS/Touch screen		
Size	Document Number	Rev
Custom	BY511/BY710	0.3
Date:	Friday, July 31, 2015	Sheet 34 of 66

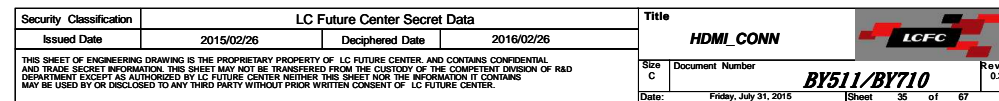


TABLE : CPU ITP DEBUG REPORT

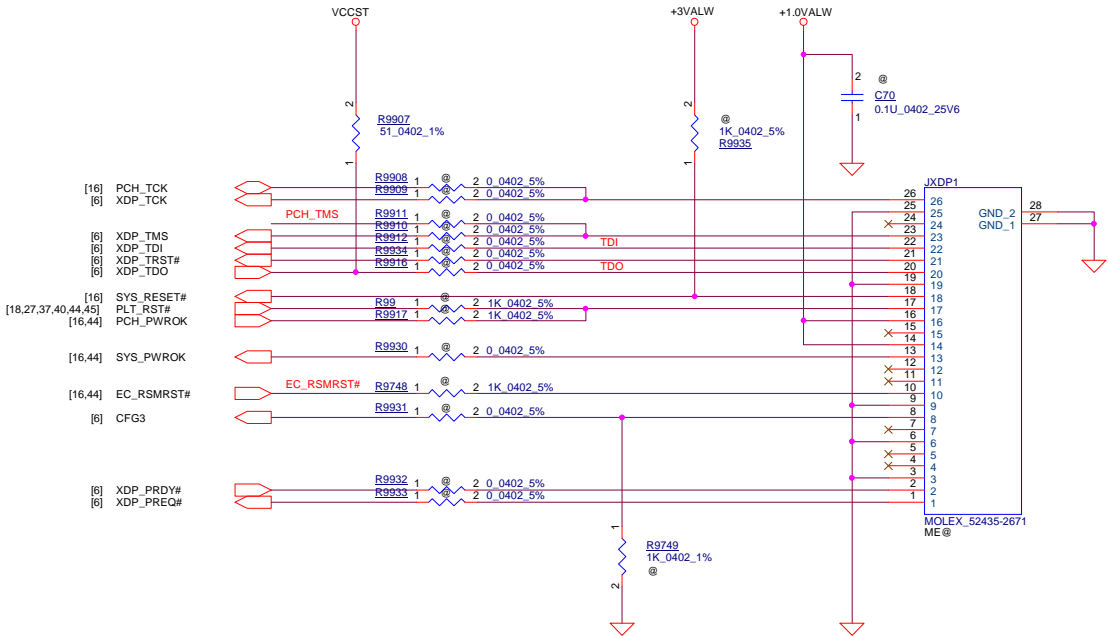
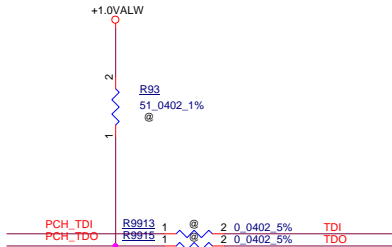
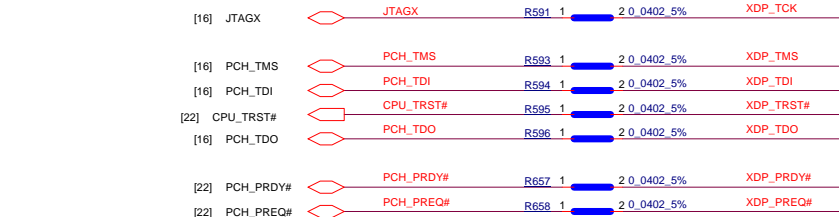
	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

TABLE : PCH ITP DEBUG REPORT

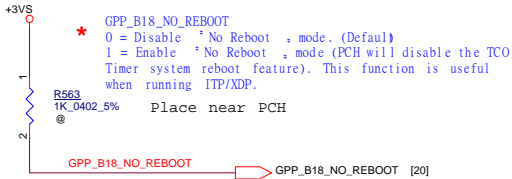
	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

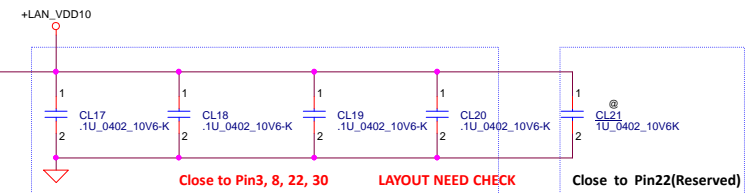
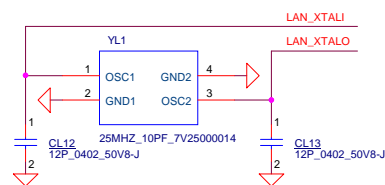
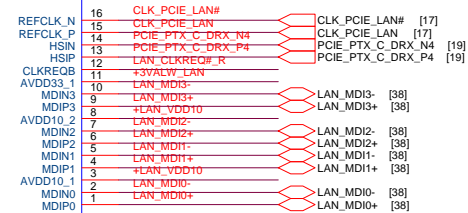
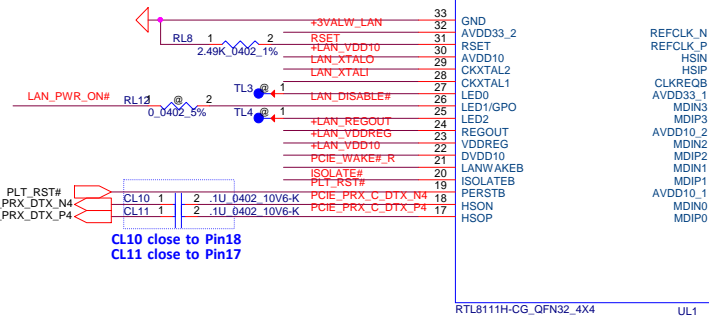
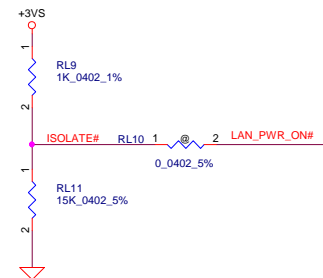
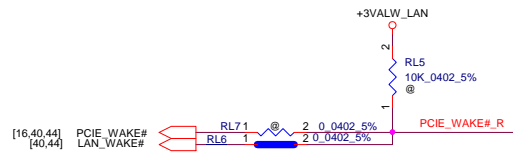
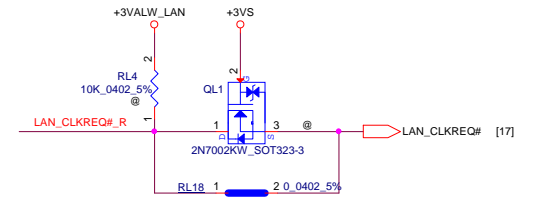
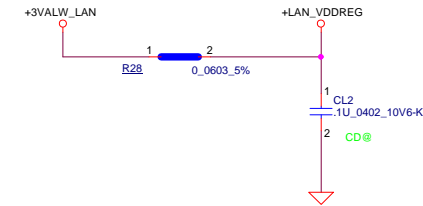
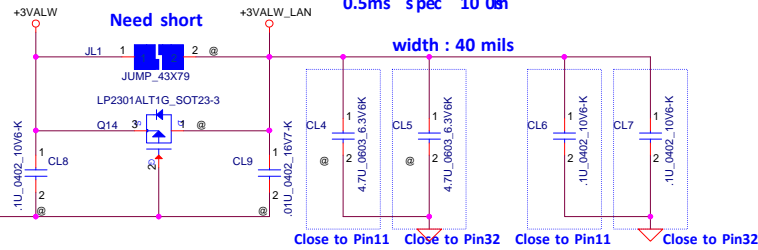
TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)			R563
HIGH	Enable "No Reboot" Mode		ASM
LOW	Disable "No Reboot" Mode (Default )		NO ASM




Reference Intel document 546884 SKL PHG

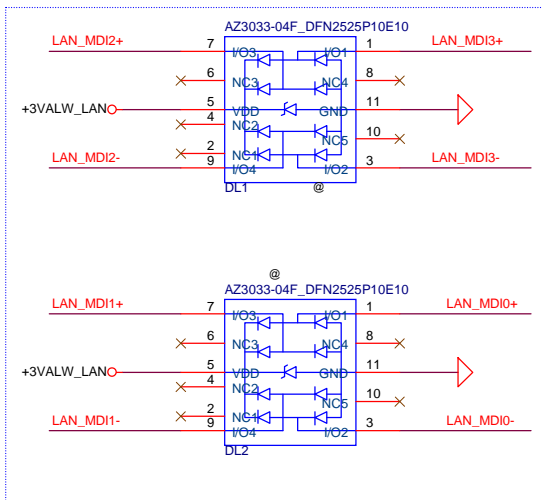




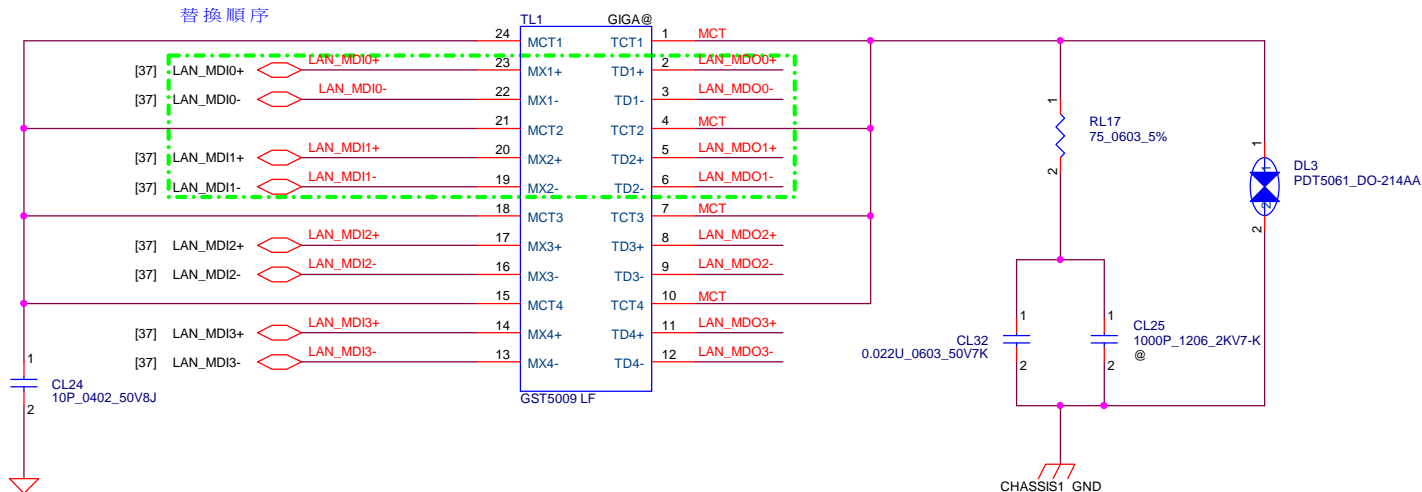
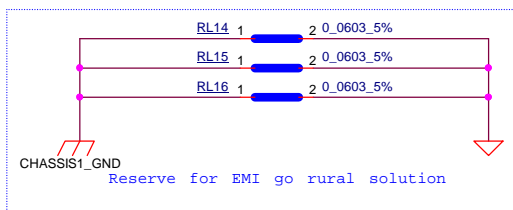
Layout Note: LL1 must be within 200mil to Pin24, CL15,CL16 must be within 200mil to LL1  
+LAN\_REGOUT: Width =60mil

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Issued Date	2015/02/26	Deciphered Date	2016/02/26	LAN_RTL8111GUL/RTL8106E 	
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				BY511/BY710	
Date:		Friday, July 31, 2015		Sheet 37	of 67

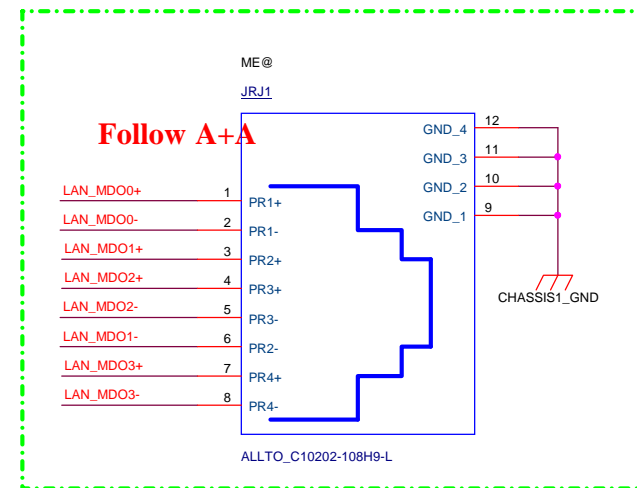
DL1/DL2  
1'S PN:SC300003M00



Place Close to TL1



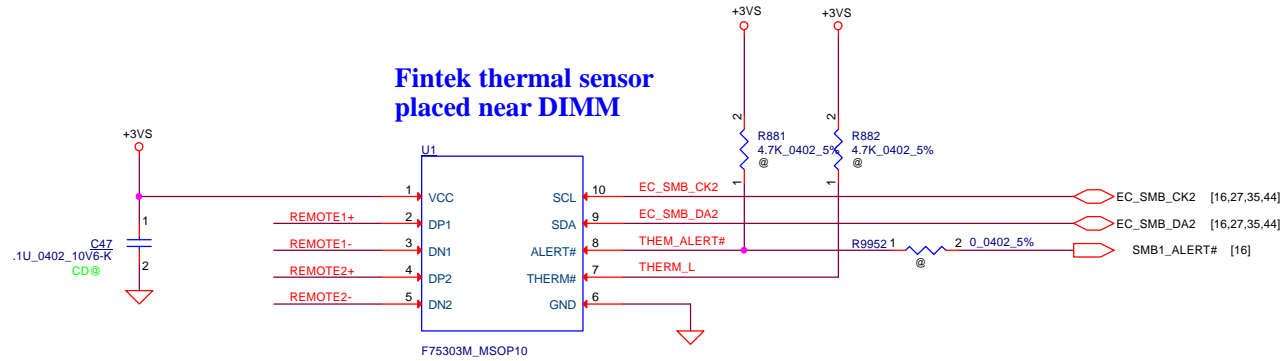
換JRJ 1 CONN



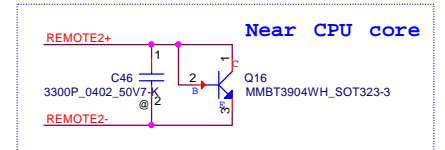
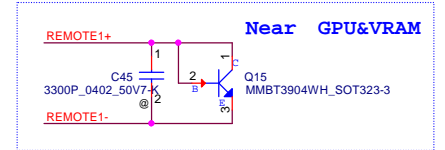
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2015/02/26	Deciphered Date	2016/02/26	LAN_Transformer	
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				Sheet	38 of 67



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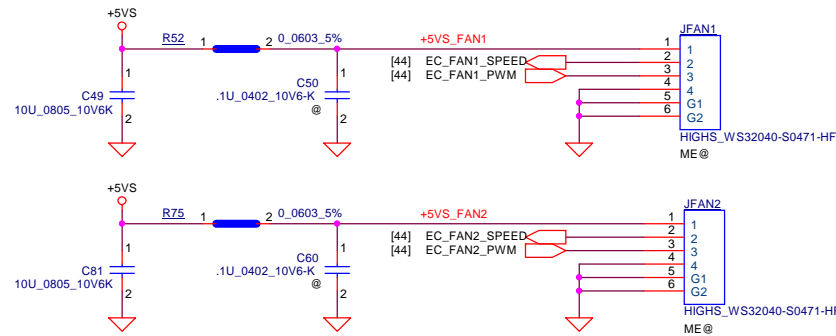


REMOTE+/-\_R, REMOTE1+/-, REMOTE2+/-:  
Trace width/space:10/10 mil  
Trace length:<8"



## FAN Conn

### Address 1001\_101xb



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				Custom	BY511/BY710
				Date:	Friday, July 31, 2015
				Sheet	39 of 66

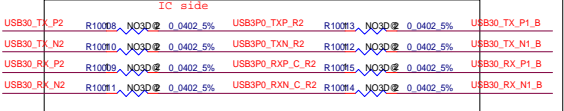
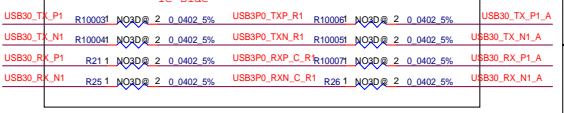
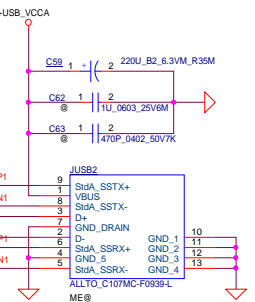
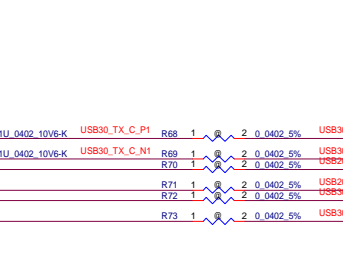
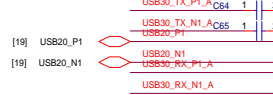
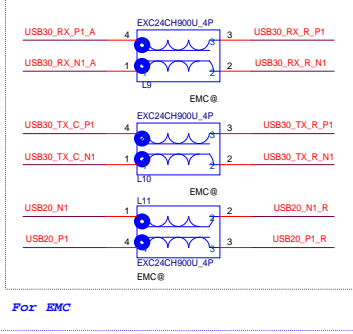
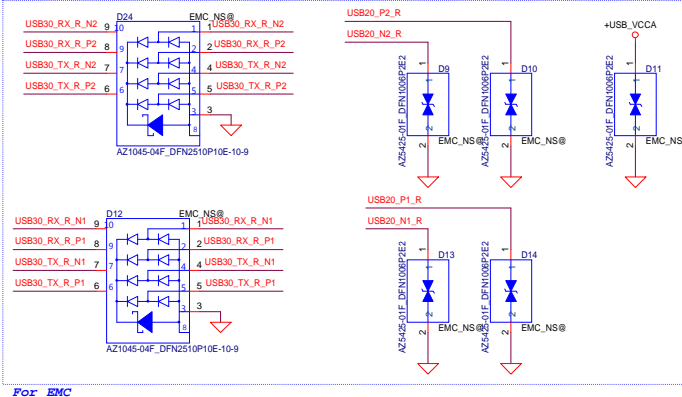
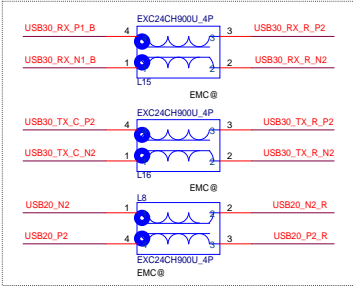
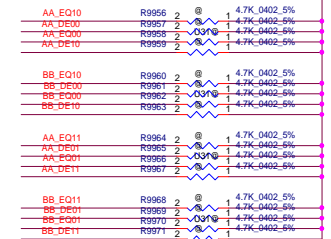
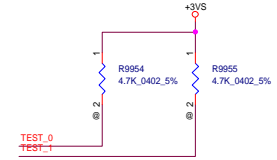
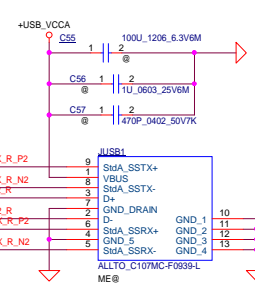
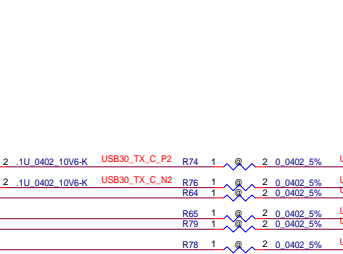
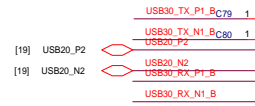
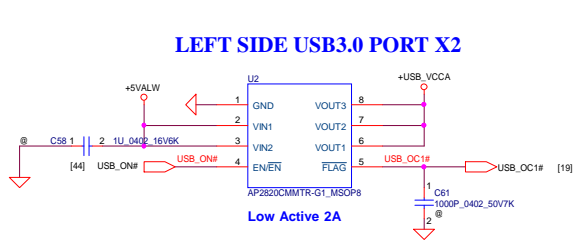


Rev 0.3

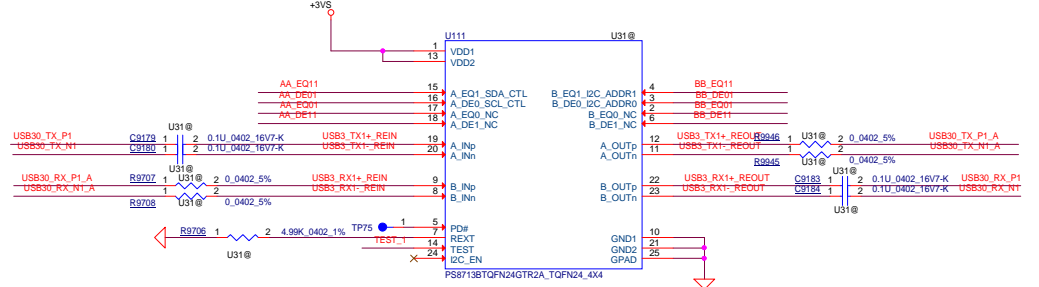




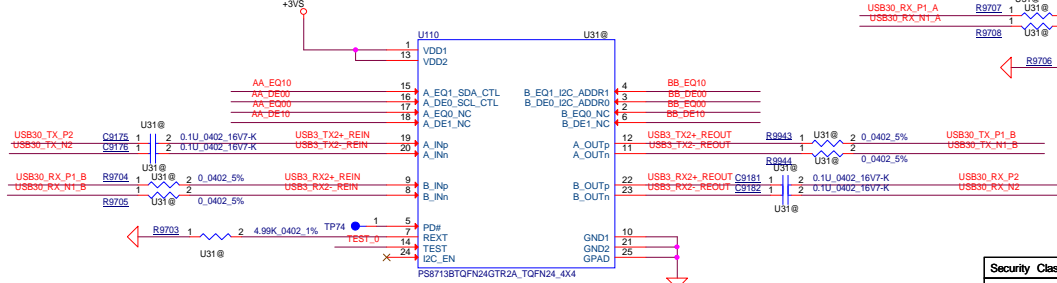
## LEFT SIDE USB3.0 PORT X2



## USB3.0 Repeater Port 2

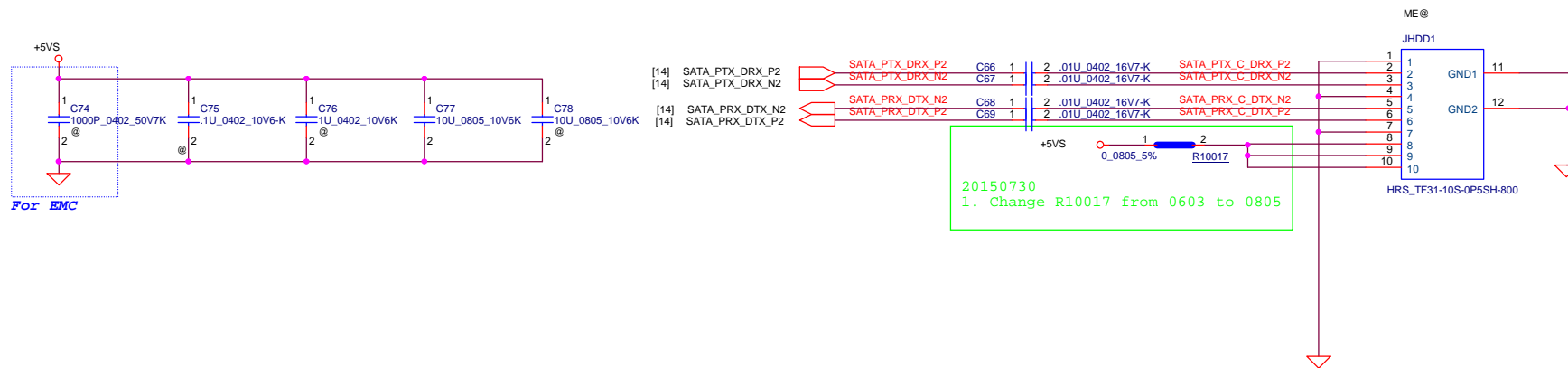


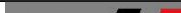
## USB3.0 Repeater Port 1

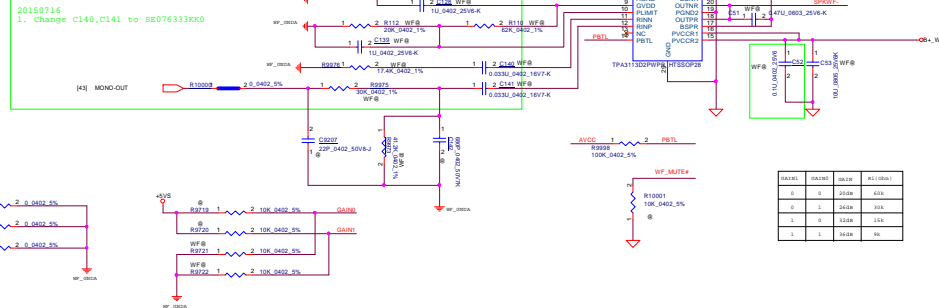
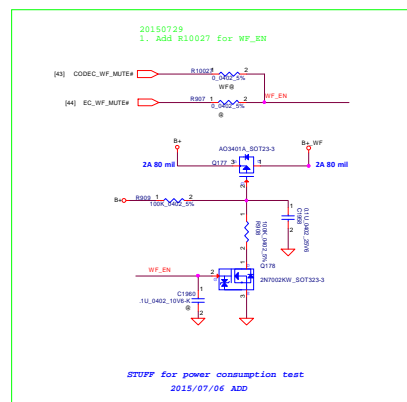
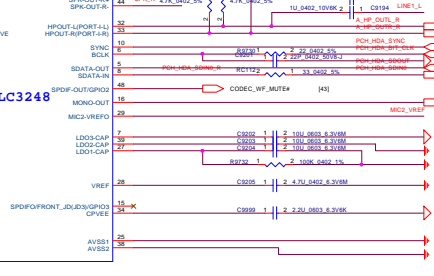
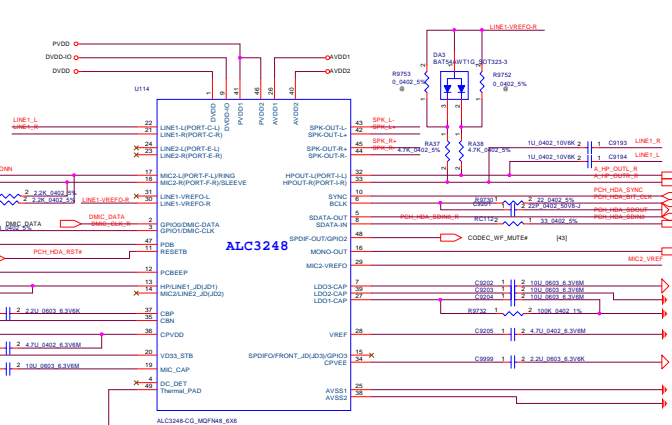
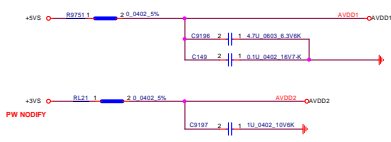


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				Friday, July 31, 2016	Sheet 41 of 66


# SATA HDD Conn.



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Size		Document		Number		Rev	
Custom				BY511/BY710		0.3	
Date:		Friday, July 31, 2015		Sheet		42 of 66	

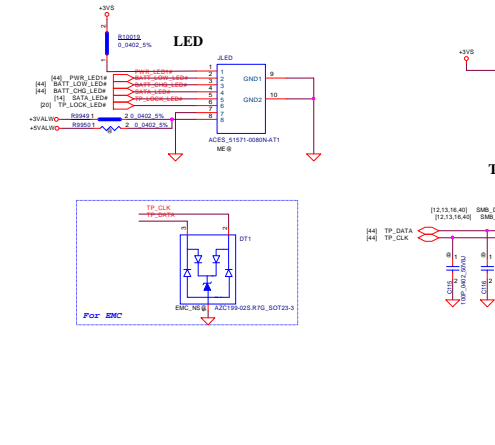


GAIN1	GAIN2	GAIN	W (GAIN)
0	0	20dB	40k
0	1	26dB	30k
1	0	22dB	15k
1	1	26dB	9k

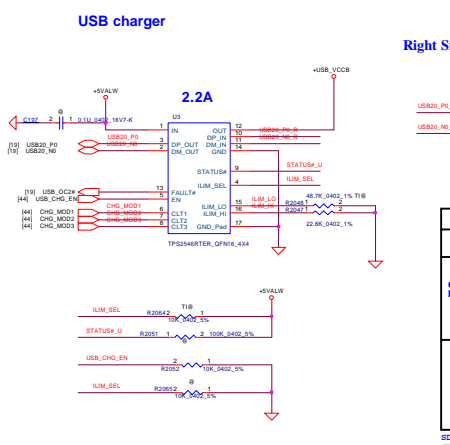
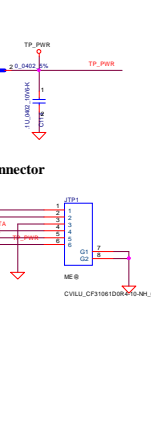
Security Classification	LC Future Center Secret Data		Title	
Issued Date	2015/02/26	Deciphered Date	2016/02/26	
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Drawn	PHONG, NGUYEN, JAMES	Checked	CS	Rev 0.1



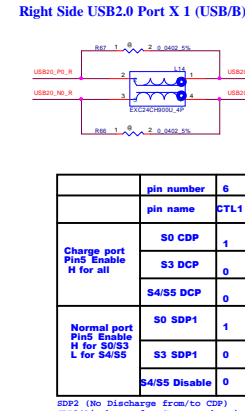
### No function field



KS0[0..17] KS0[0..17] [44]



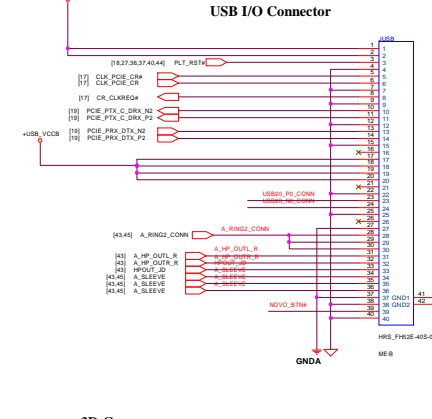
A circuit diagram showing a single resistor. The resistor is represented by a zigzag line. Above the resistor, the value "0.0402 5%" is displayed. The resistor is connected in a simple loop circuit.



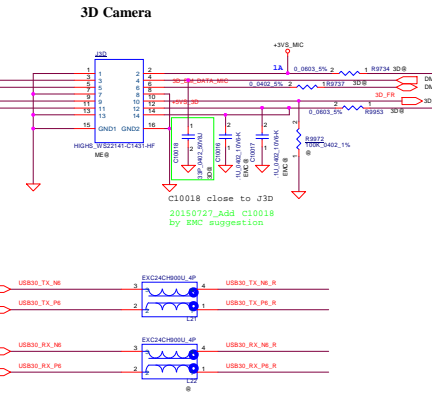
	pin number	6	7	8	4
	pin name	CTL1	CTL2	CTL3	ILM SE
Charge port Pin5 Enable H for all	S0 DCP	1	1	1	1
	S3 DCP	0	1	1	0/1
	S4/S5 DCP	0	0	1	0/1
Normal port Pin5 Enable H for S0/S3 L for S4/S5	S0 SDP1	1	1	0	0/1
	S3 SDP1	0	1	0	0/1
	S4/S5 Disable	0	0	0	0/1

SDP2 (No Discharge from/to CDP)  
SDP1(Discharge from/to any charging state including CDP)

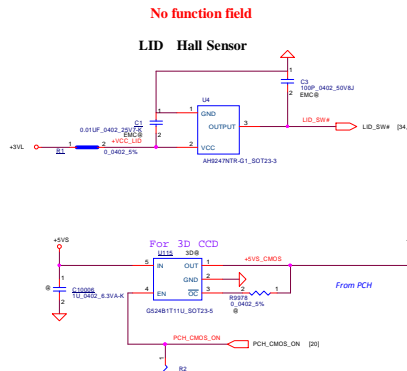
Diagram of a 3-bit shift register. The inputs are labeled D, Q2, Q1, and Q0. The outputs are labeled Q2, Q1, and Q0. A red box highlights the D input of the first flip-flop and the Q2 output of the second flip-flop.



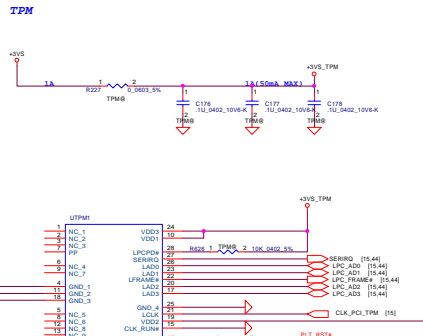
150




## L1D Hall Sensor



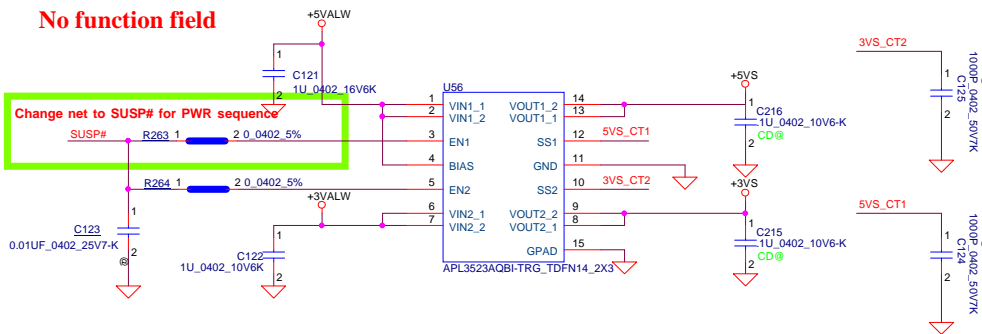
4SVS



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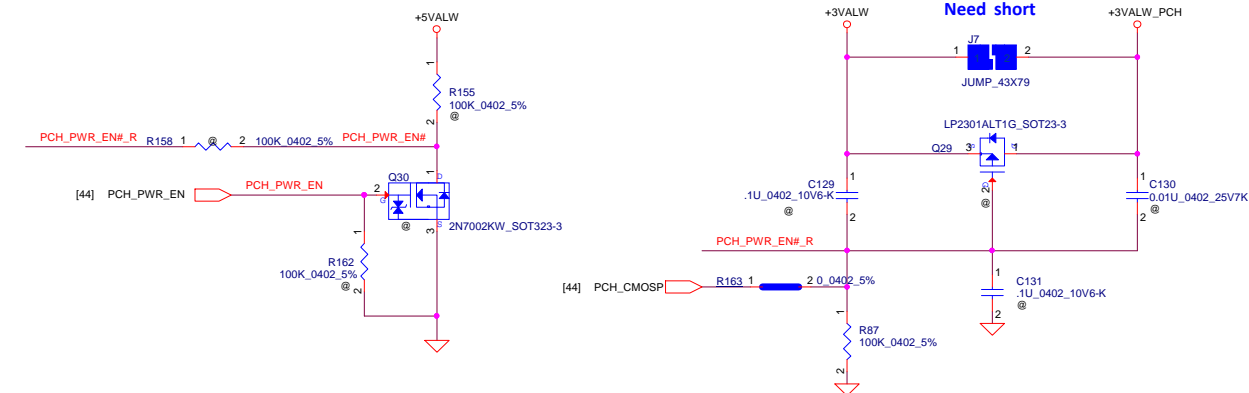
+5VALW to +5VS

No function field

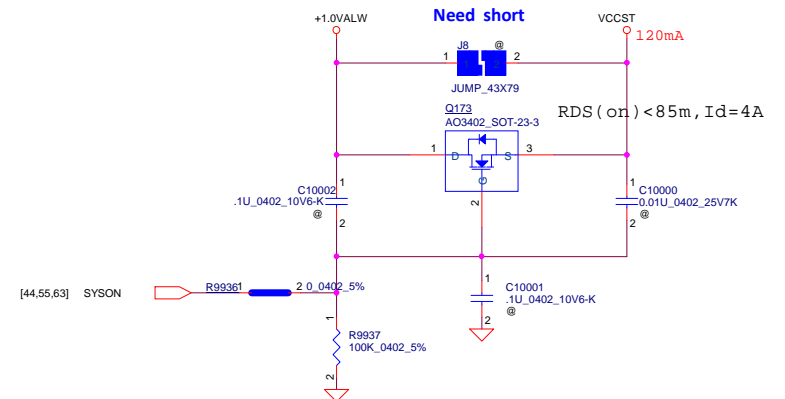


LP2301ALT1G  
Rds=110mohm @  
VGS=4.5V, ID=2.8A  
VGS(th)=1V Max

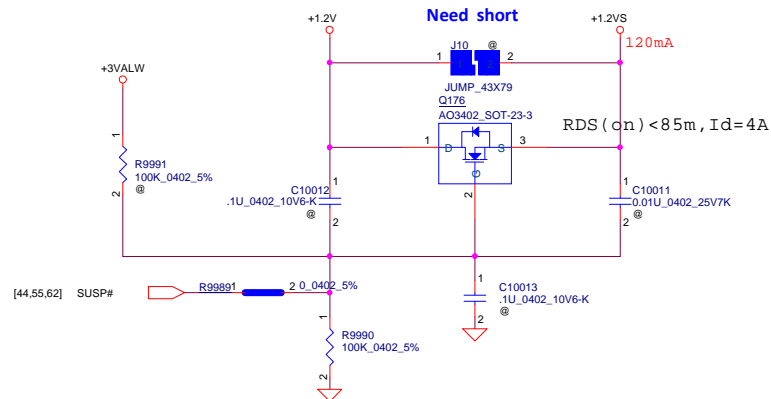
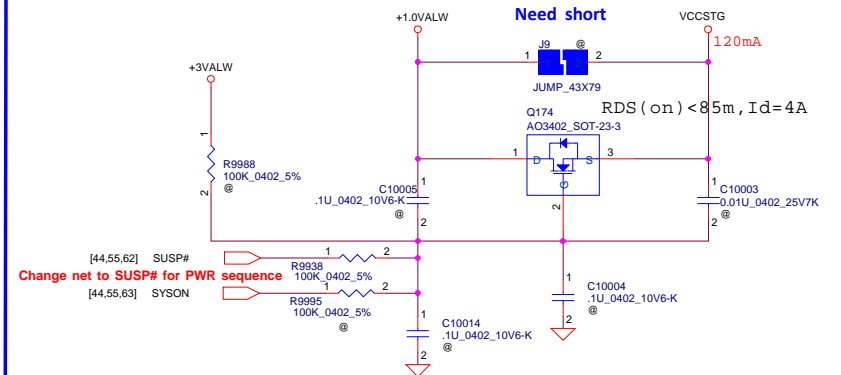
Need short



Need short

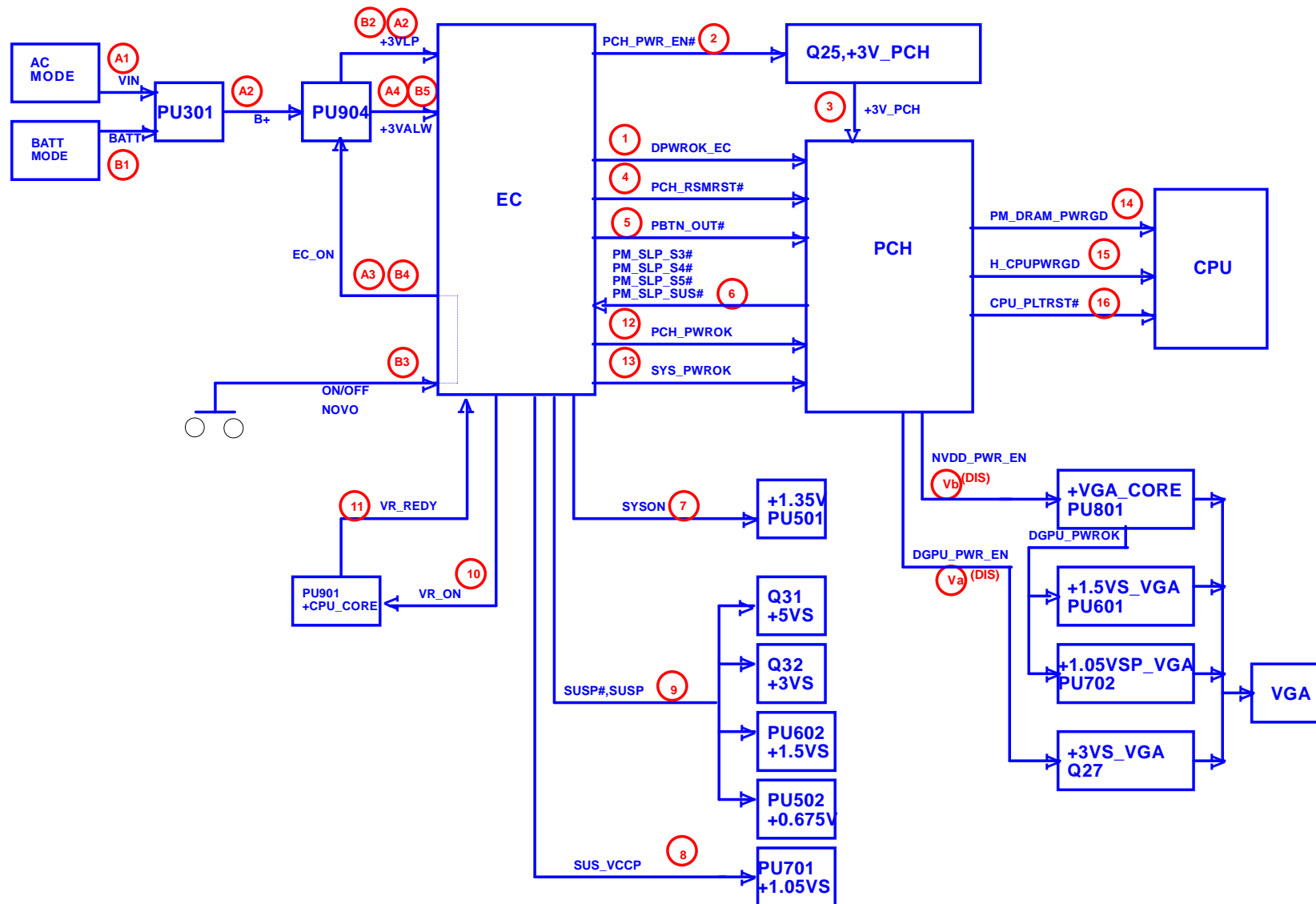


Need short



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D

1

C


1

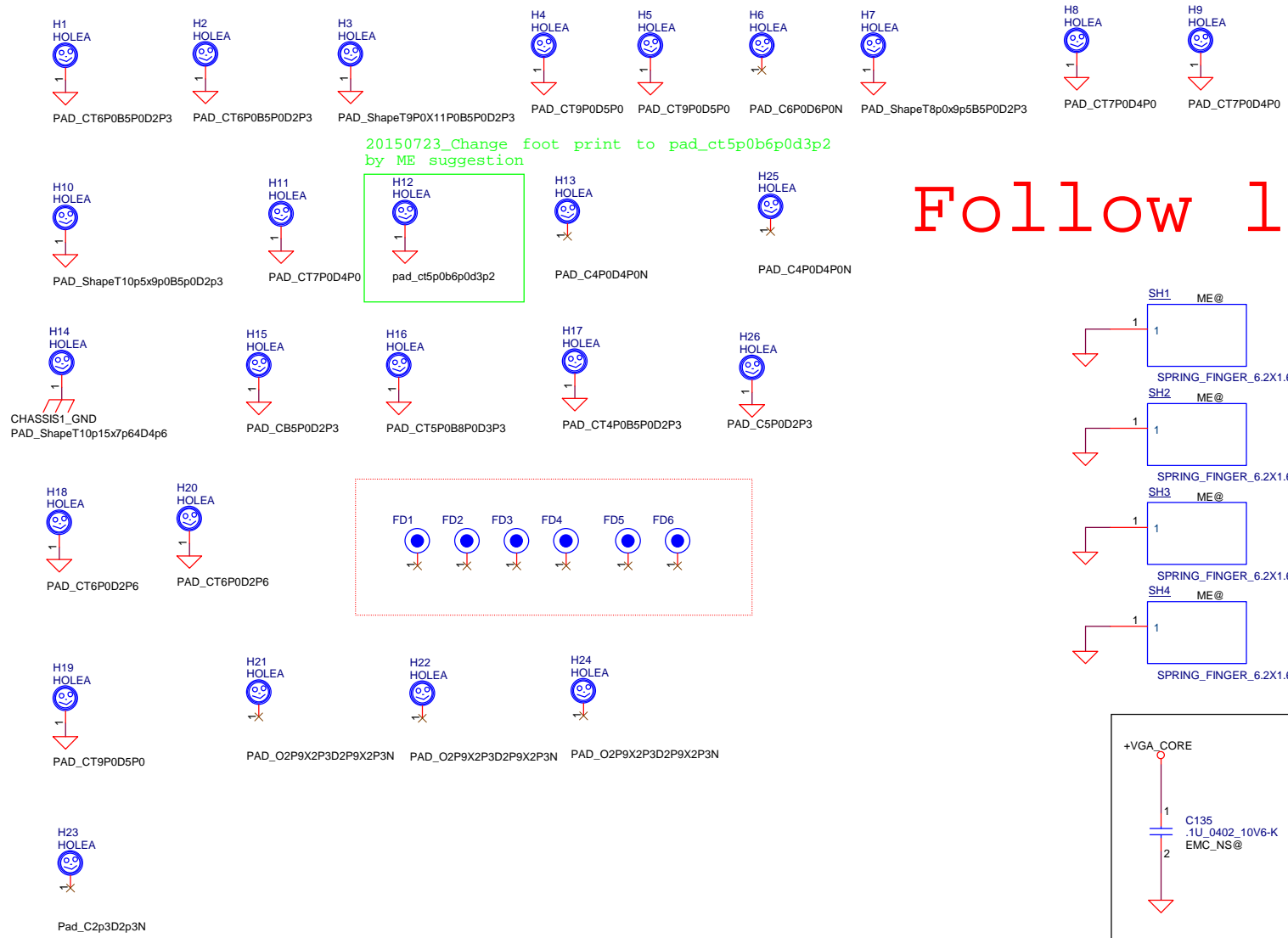
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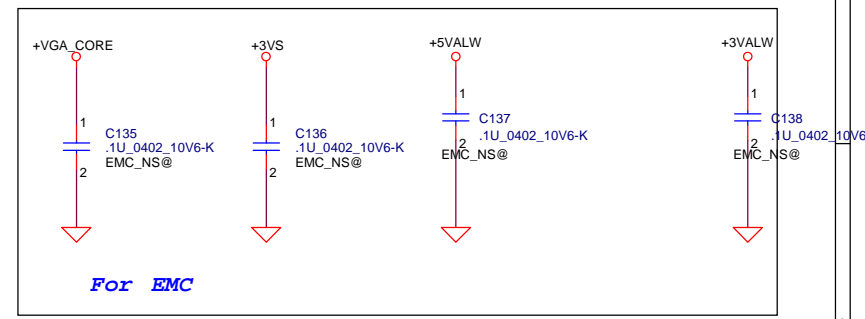
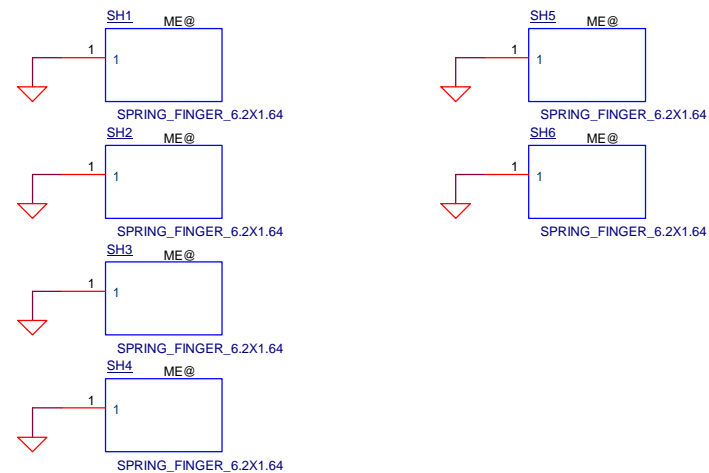
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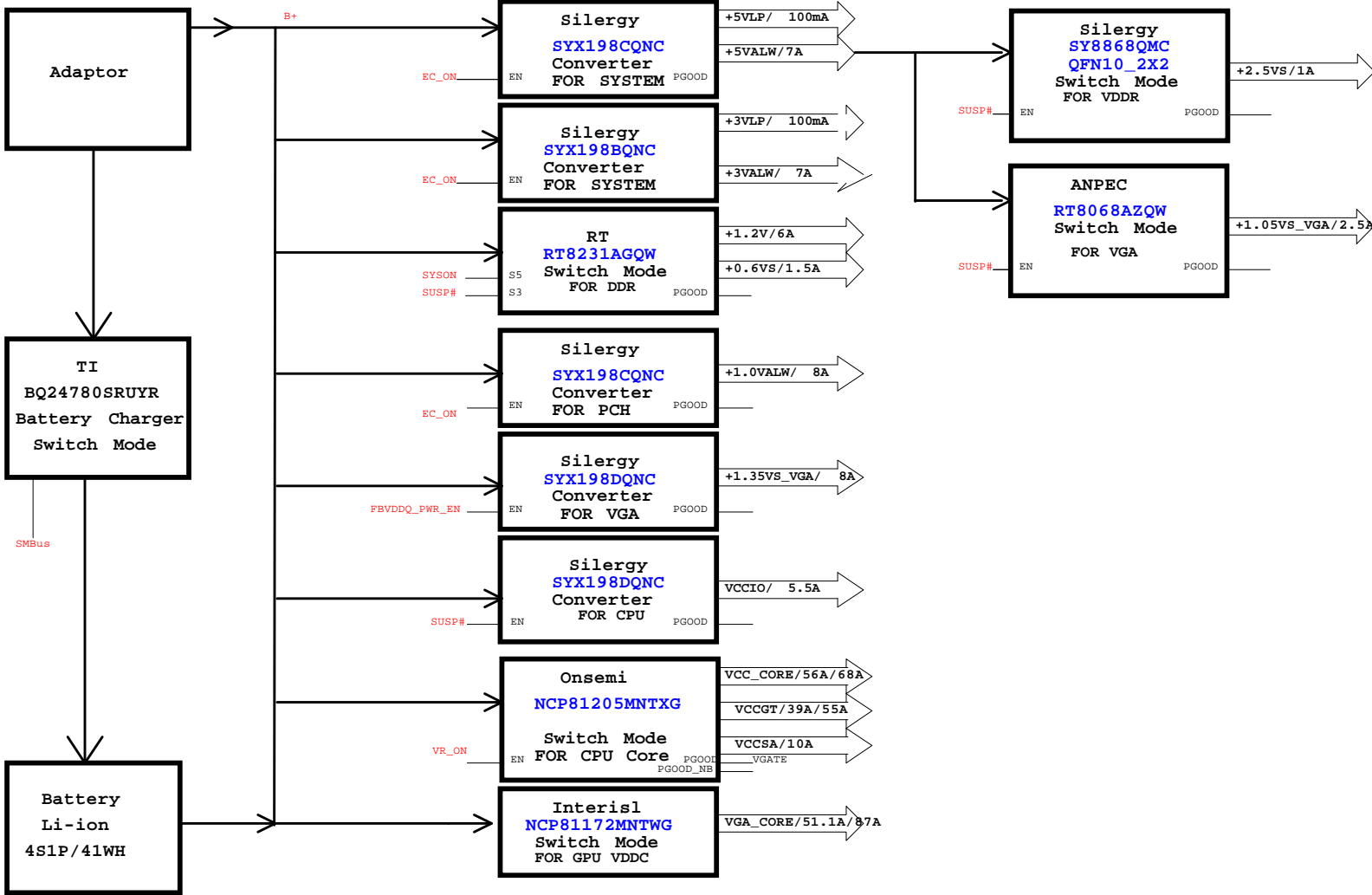
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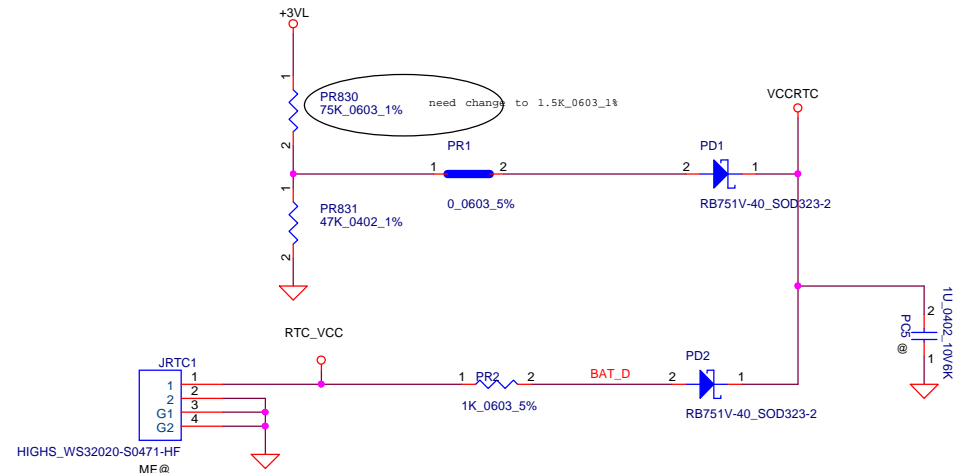
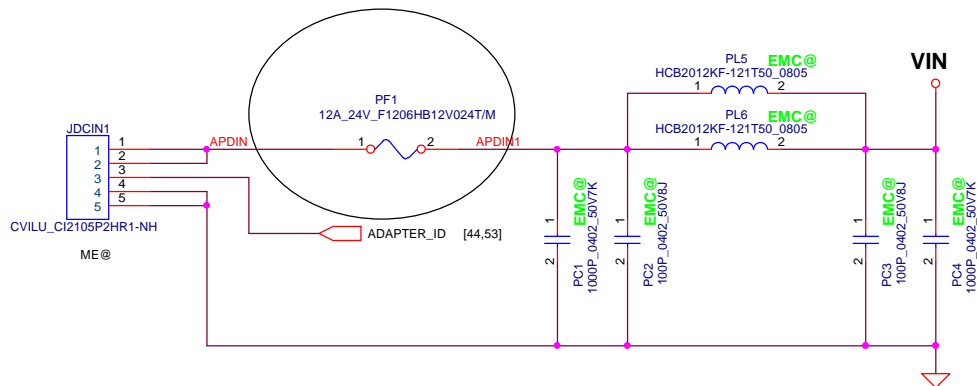
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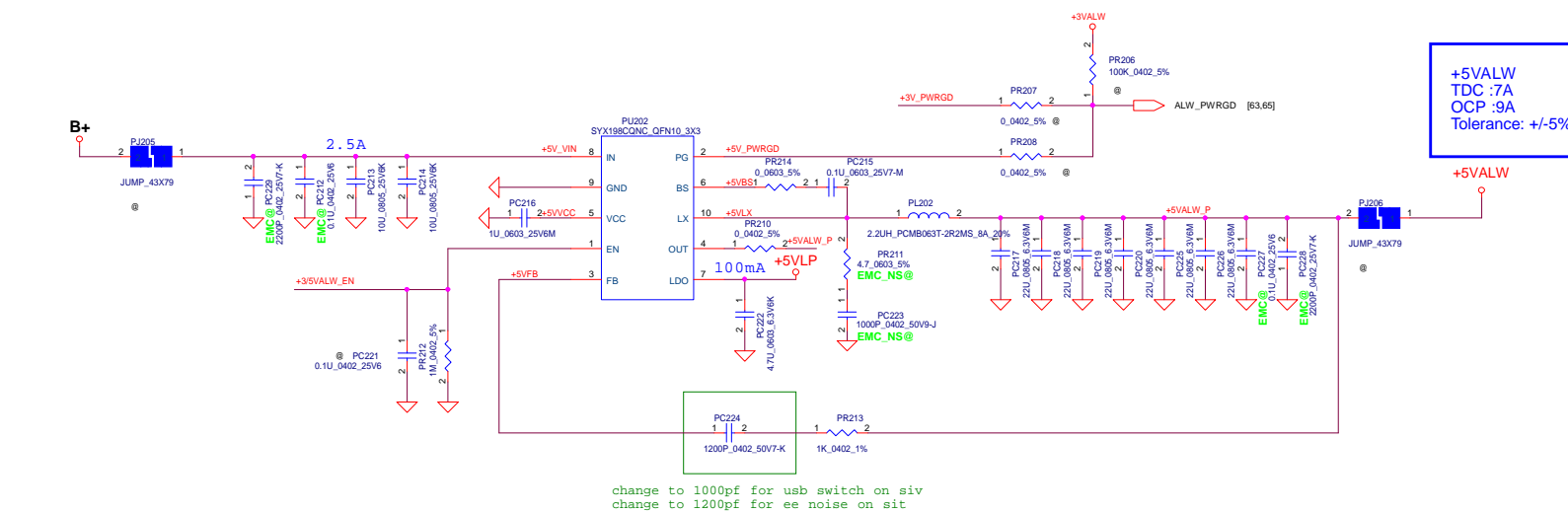
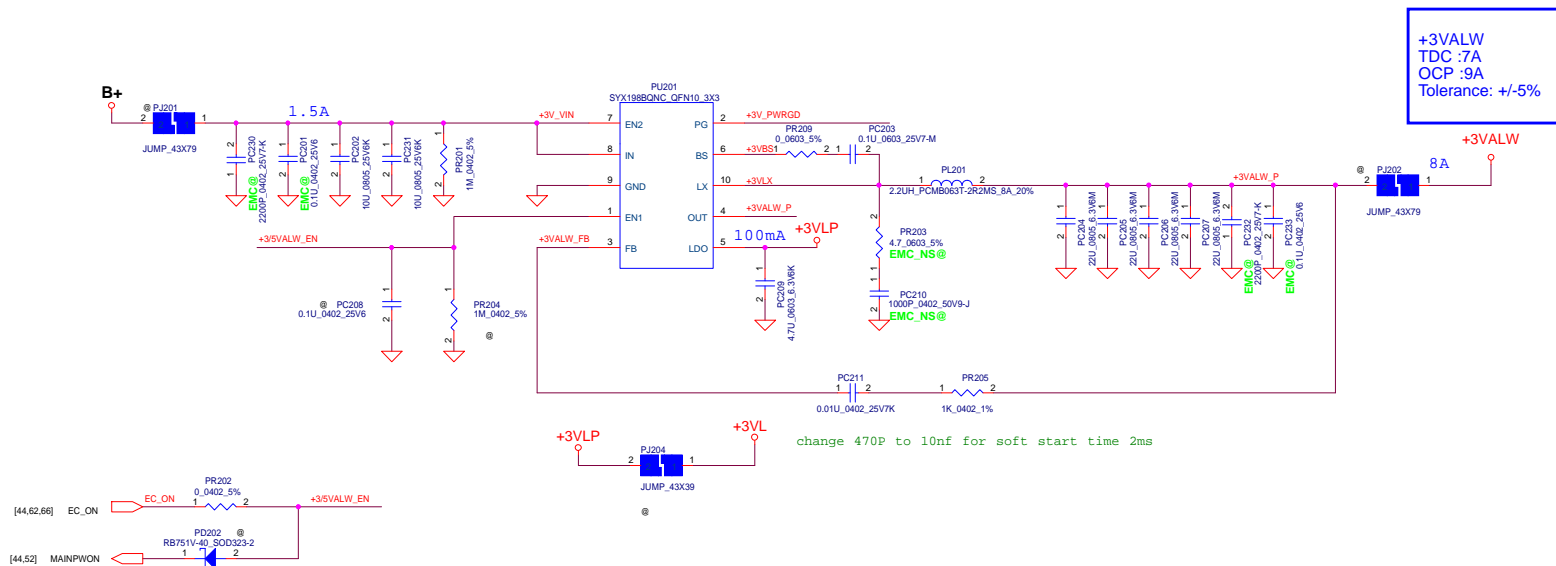


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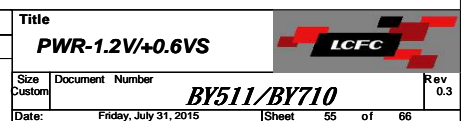
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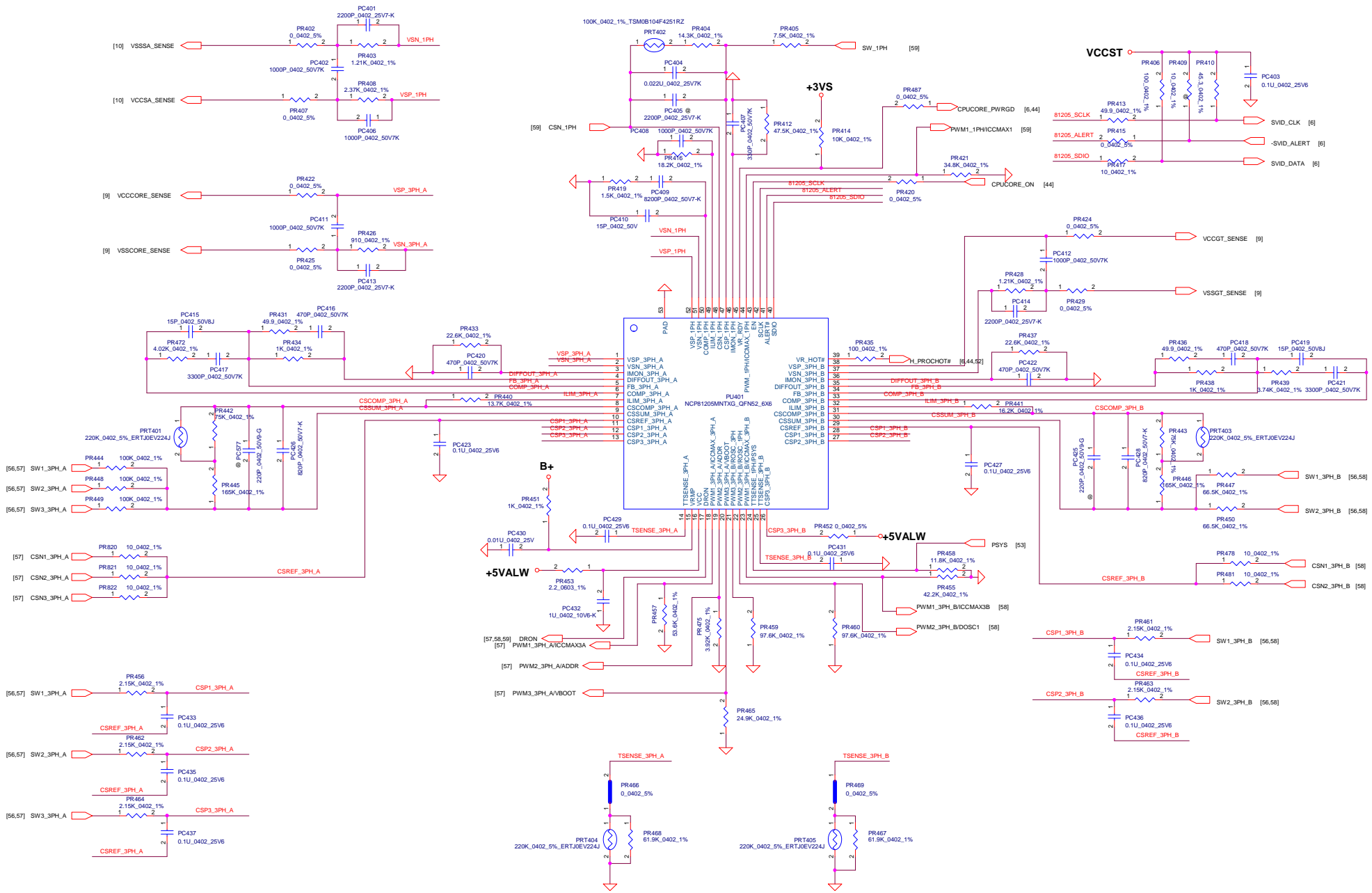


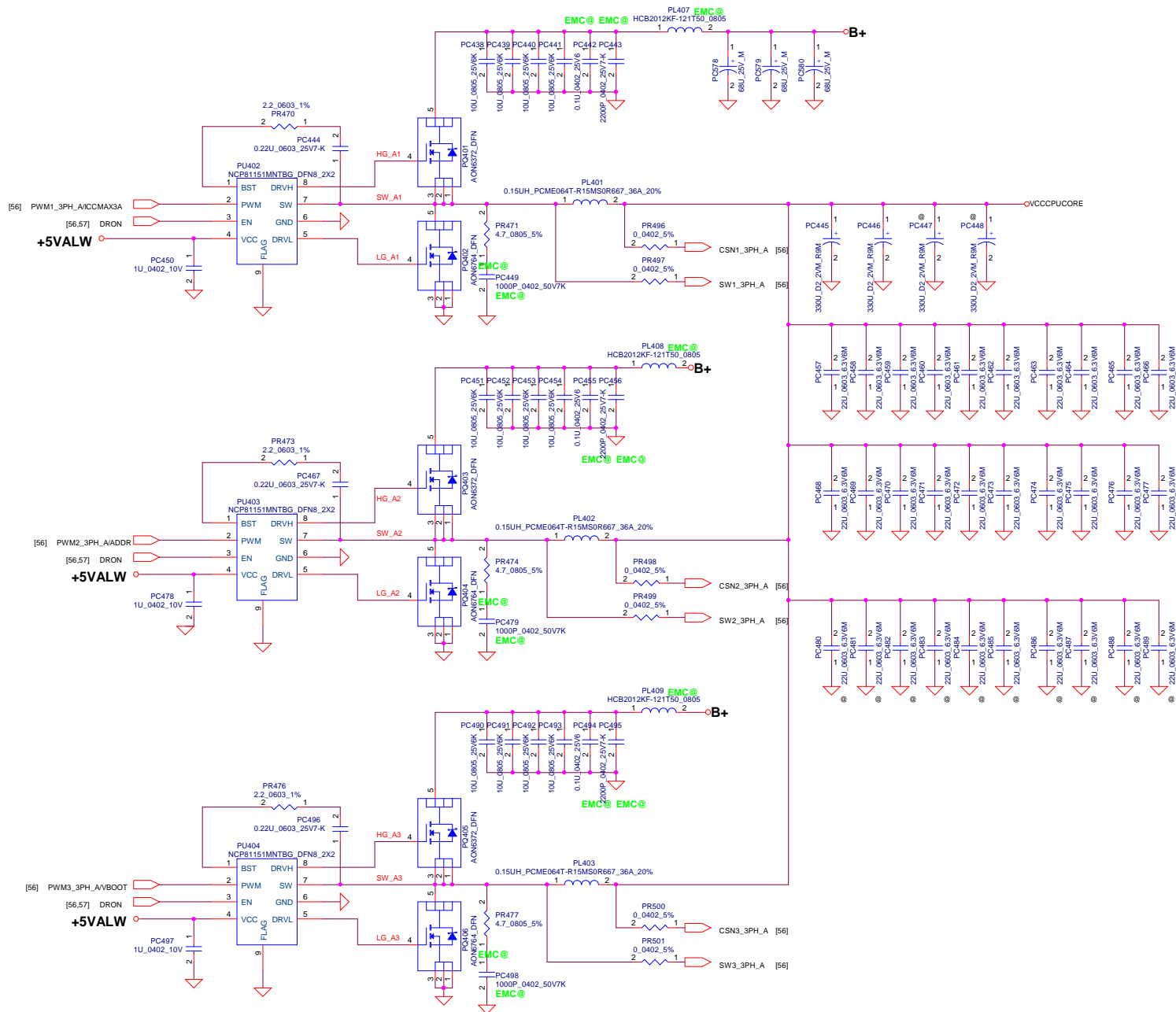







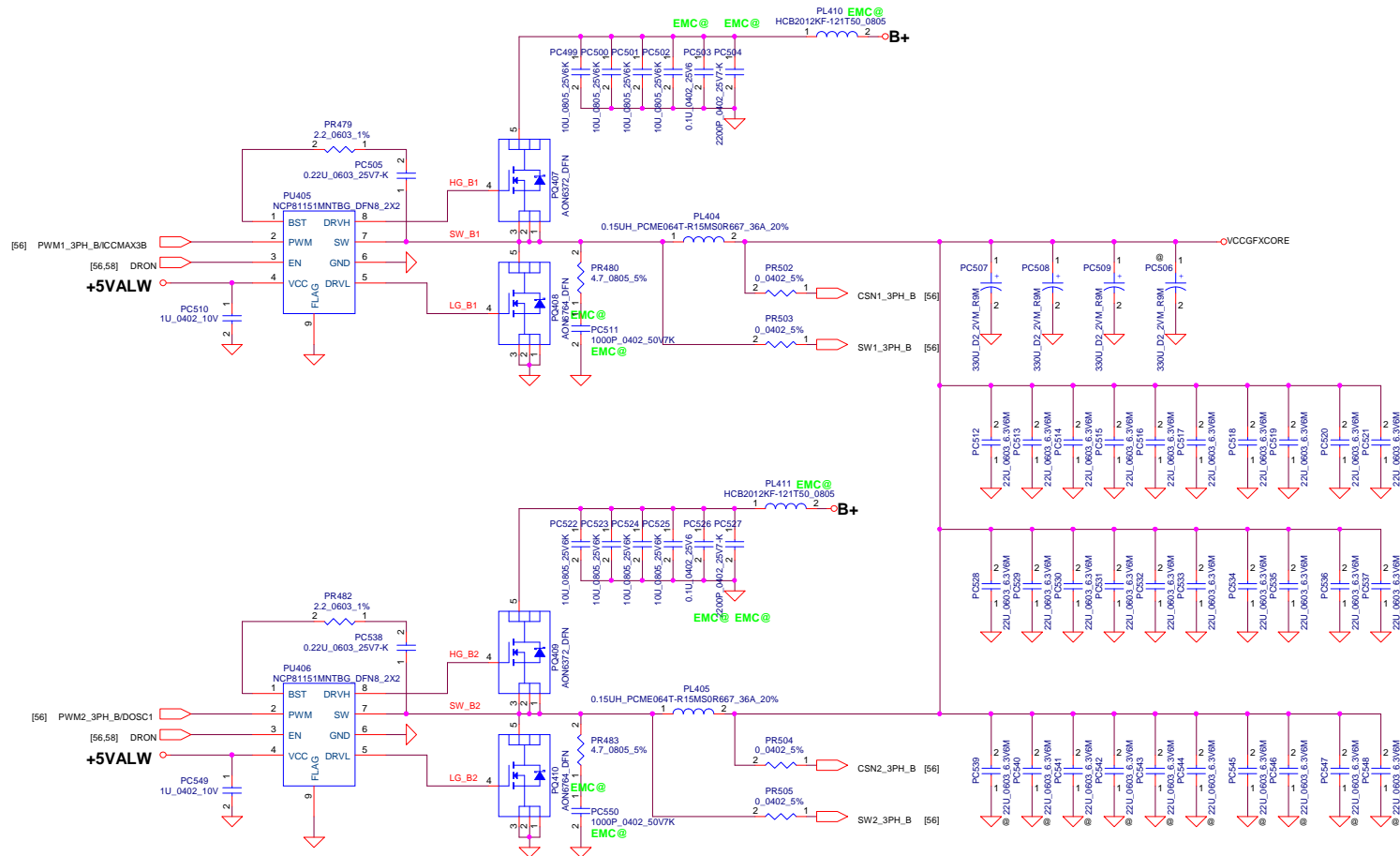







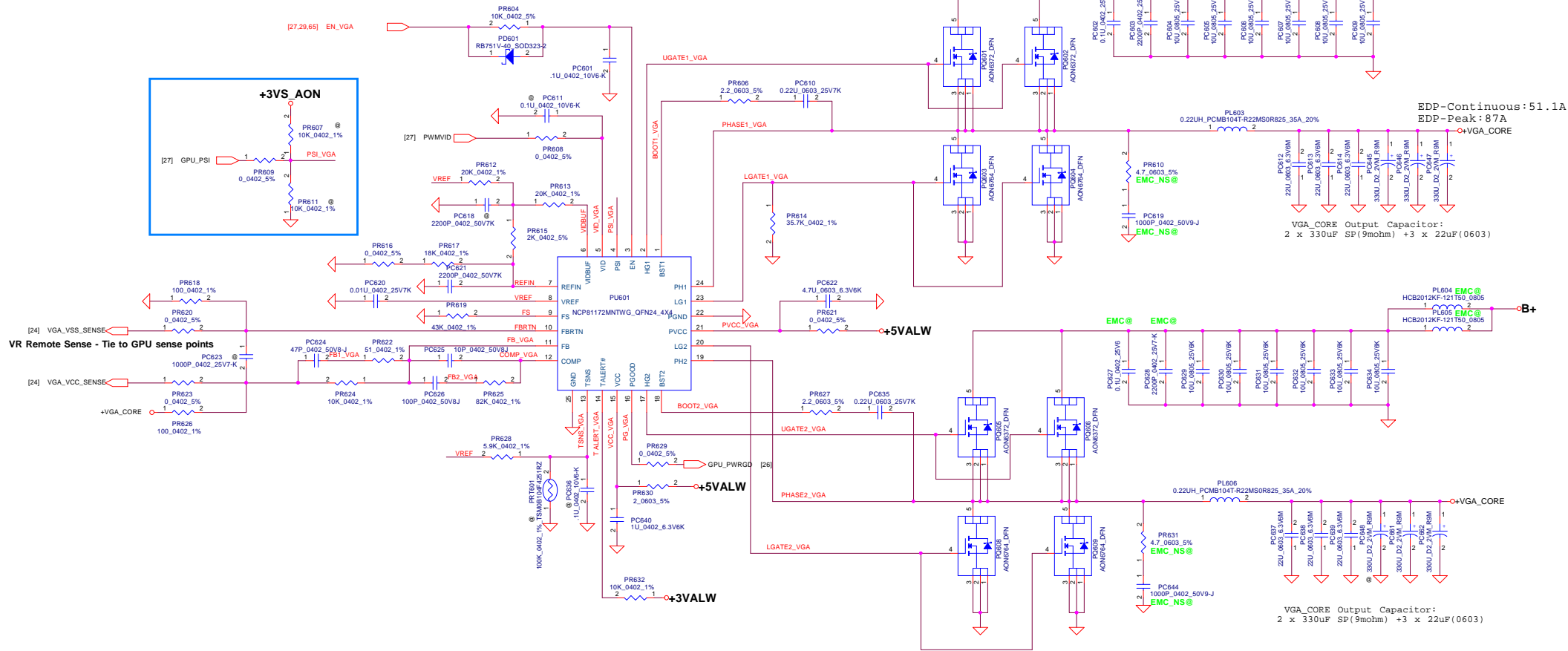
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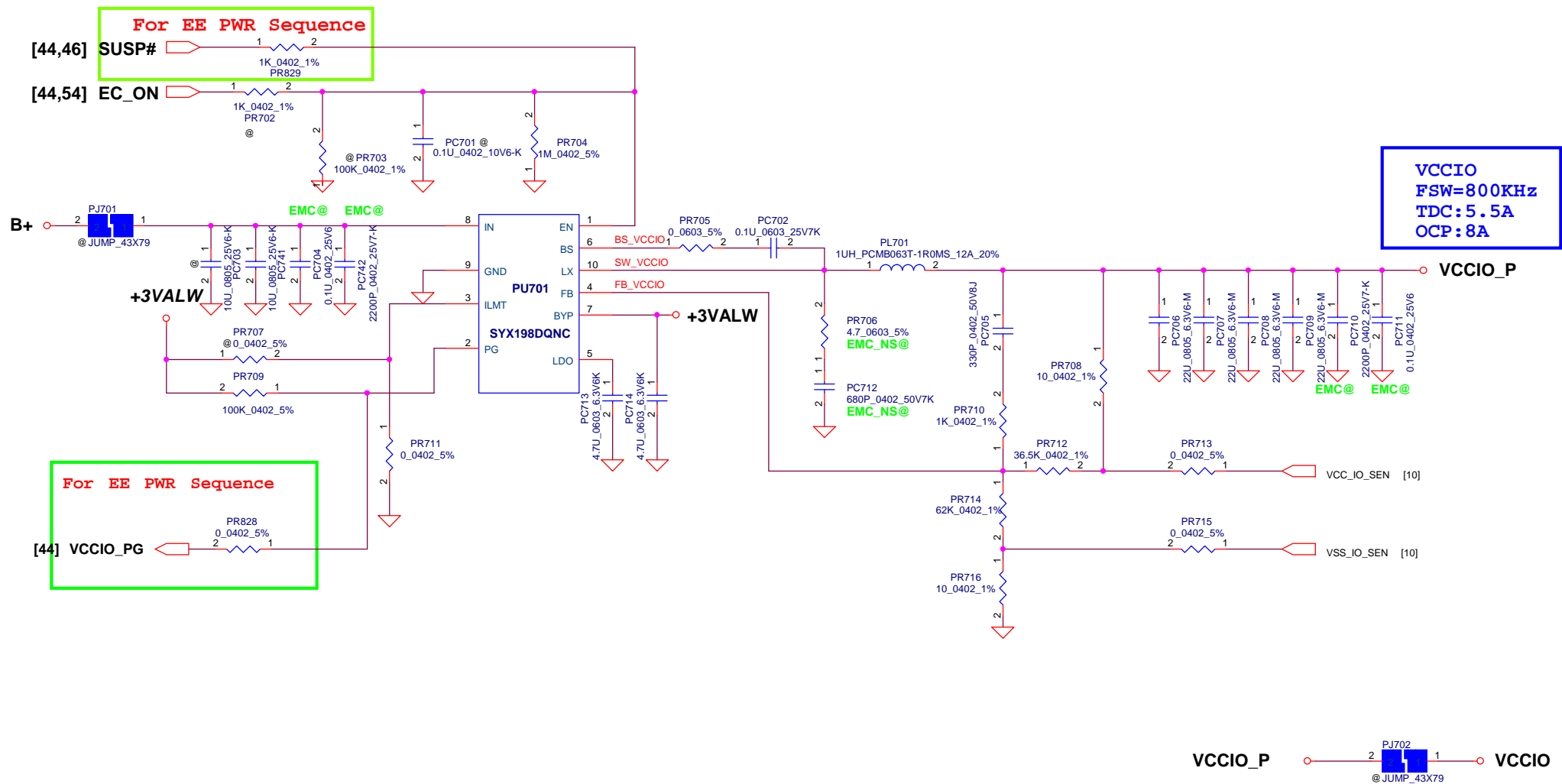
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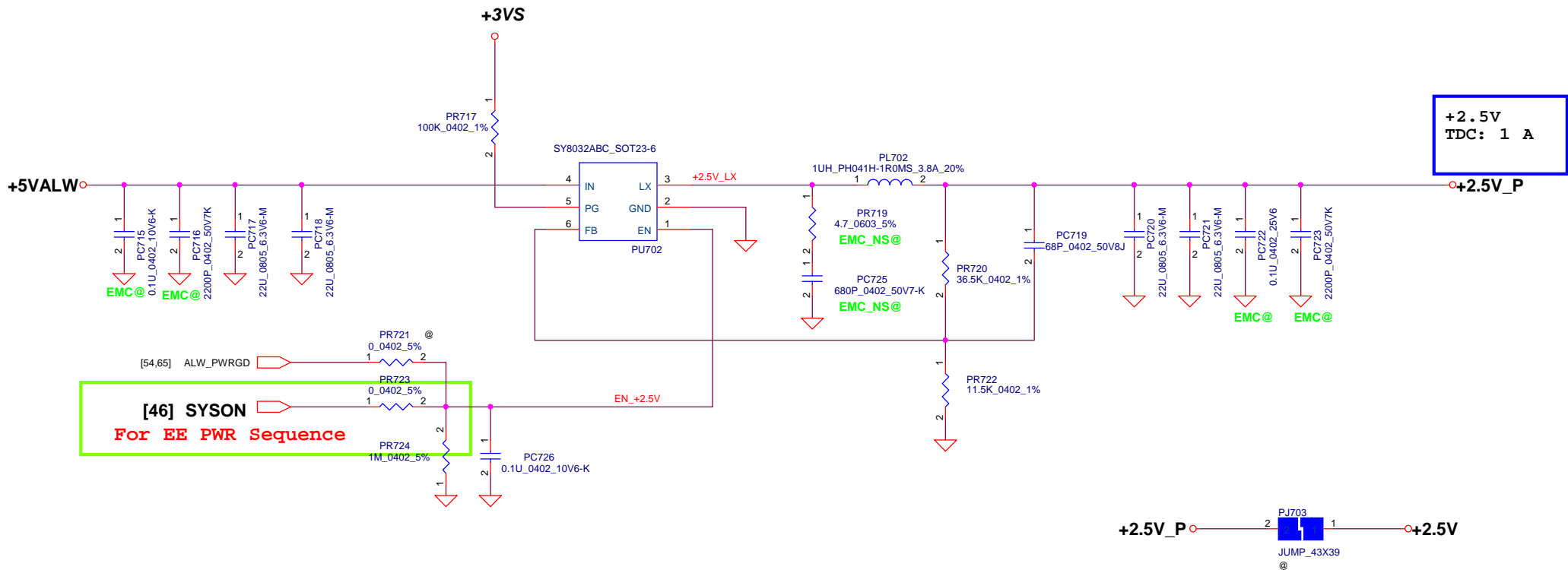




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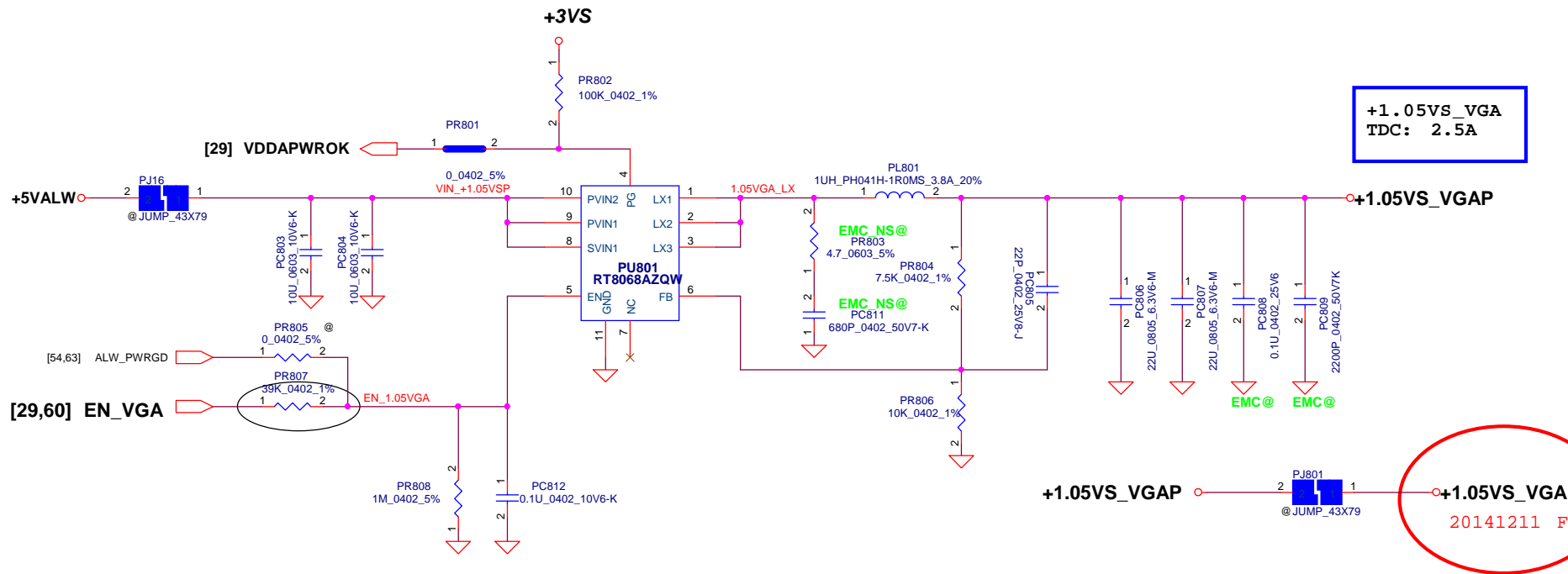



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